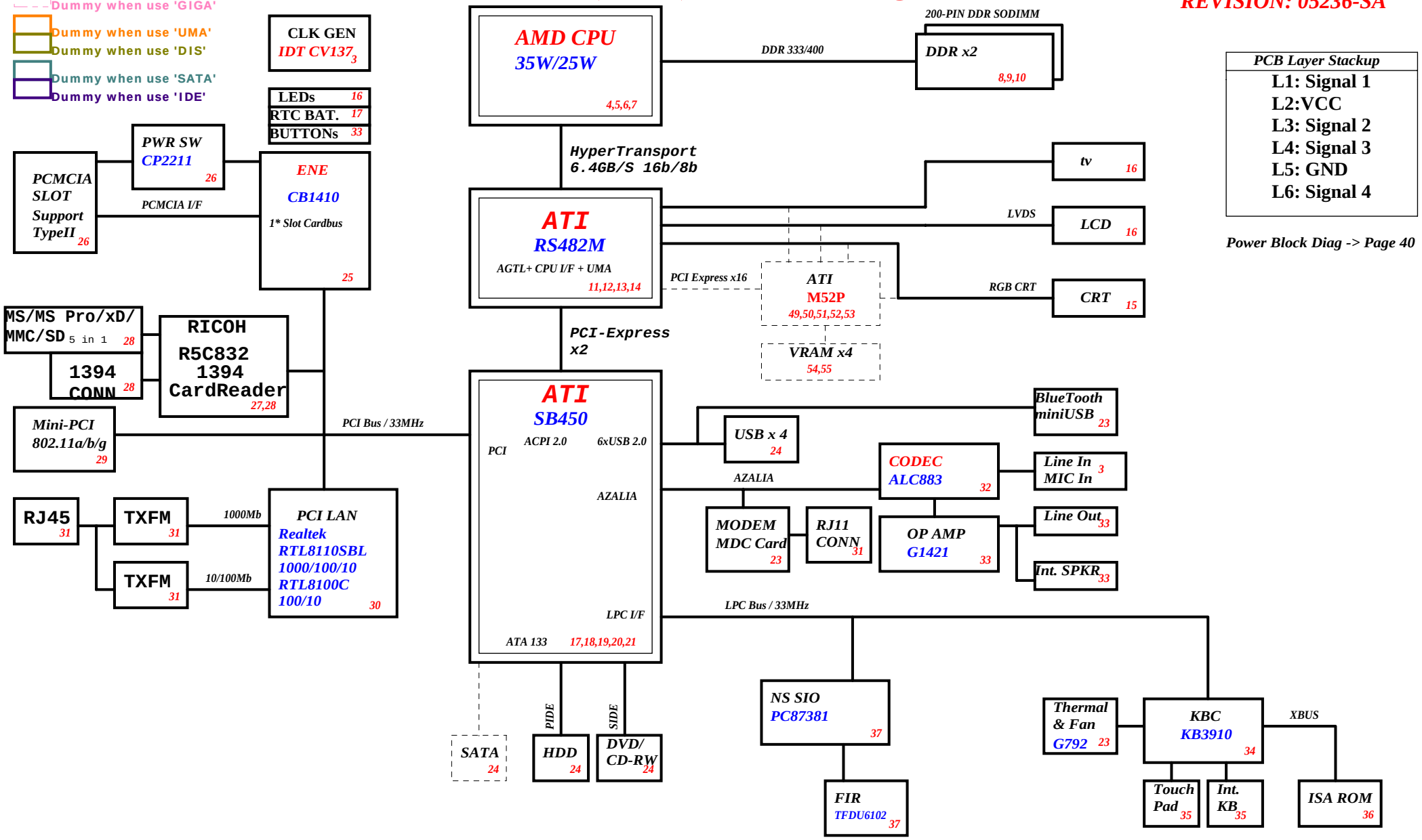
See 'TEXT' in 0MEMO or 1MEMO property in component

Bolsena-E(AB2) Block Diagram

Project Code: 91.4G401.001
REVISION: 05236-SA

Dummy when use '10/100'
Dummy when use 'GIGA'
Dummy when use 'UMA'
Dummy when use 'DIS'
Dummy when use 'SATA'
Dummy when use 'IDE'



PCB Layer Stackup
L1: Signal 1
L2:VCC
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

Power Block Diag -> Page 40

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 1 of 58

PCI Routing

	IDSEL	IRQ	REQ/GNT
MiniPCI	21	F	0
LAN	23	H	2
7411	22	E (CardBus)	1
7411	17	G (1394)	3
7411	17	E (FlashMedia)	3

```
Ref.  function    schematic         BOM
-------------------------
U81  cpu socket    62.10055.121  (DON'T CHANGE)  (3mm high)
U80  north bridge  71.RS482.M03  71.RS482.M03  (ver A12)
U43  south bridge  71.SB400.B0U  71.SB400.D0U  (ver A13)
U32  clock gen.    71.00137.C0W  71.00137.C0W

---
U70  VGA M52     71.0M52P.A0U
U64  VRAM FOR M52
U65  VRAM FOR M52
U69  VRAM FOR M52
U71  VRAM FOR M52





---
U66  BIOS SOCKET  72.39040.G03  62.10002.032   (NO NEED WHEN PD)
U66  BIOS IC      72.39040.G03  72.39040.H03  (DIP STAGE IN LAB, SMT IN PD)
---
U75  GIGA LAN    71.08110.00G  71.08110.A0G
U75  10/100 LAN  71.08110.00G  71.08100.C0G
```

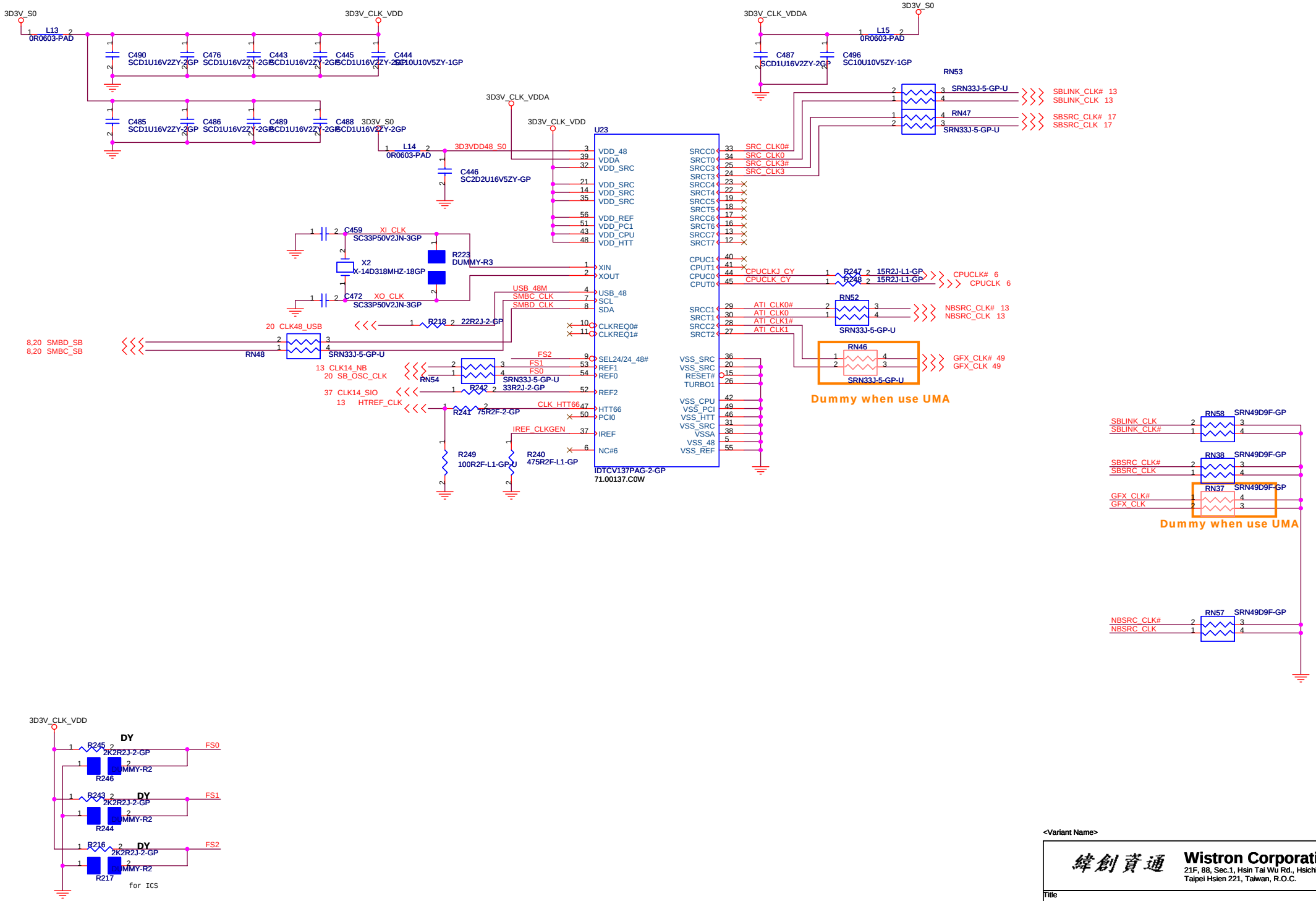
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HISTORY

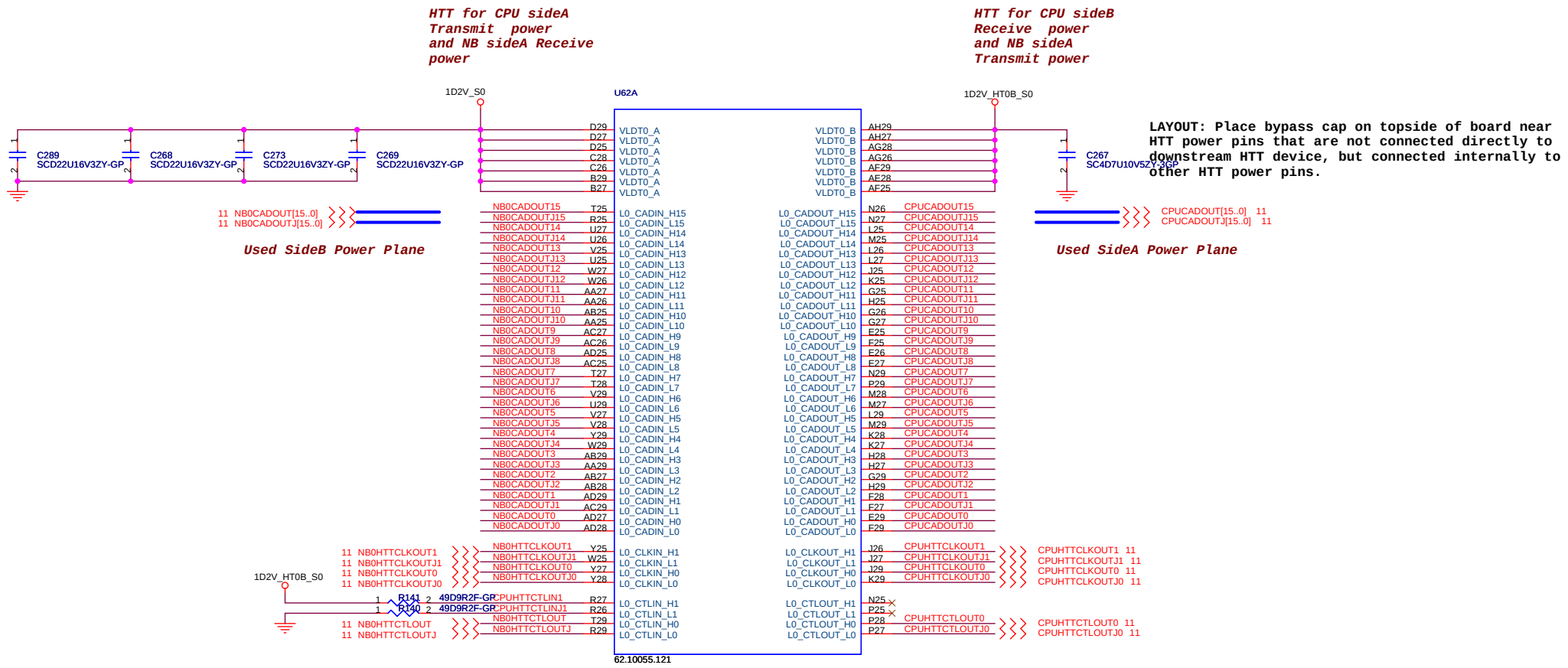
Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 2 of 58



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CLKGEN_IDTCV137**	
Size A3	Document Number **Bolsena-E**	Rev SA
Date: Thursday, October 13, 2005	Sheet 3 of 58	



LAYOUT: Place bypass cap on topside of board near HTT power pins that are not connected directly to downstream HTT device, but connected internally to other HTT power pins.

ME : 62.10055.121
2nd:62.10055.101

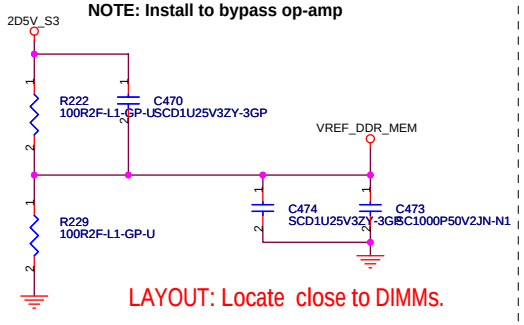
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CPU(1/4)_HyperTransport I/F**
Size A3	Document Number **Bolsena-E** Rev SA
Date: Thursday, October 13, 2005	Sheet 4 of 58

VREF_DDR_MEM

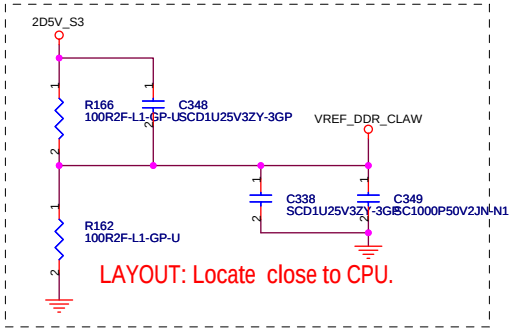
NOTE: Test with passive probes only.

NOTE: Install to bypass op-amp

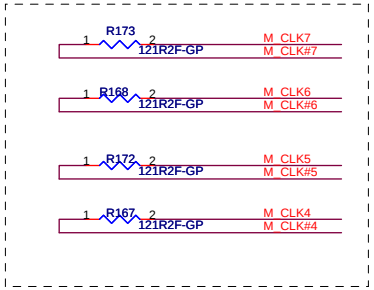


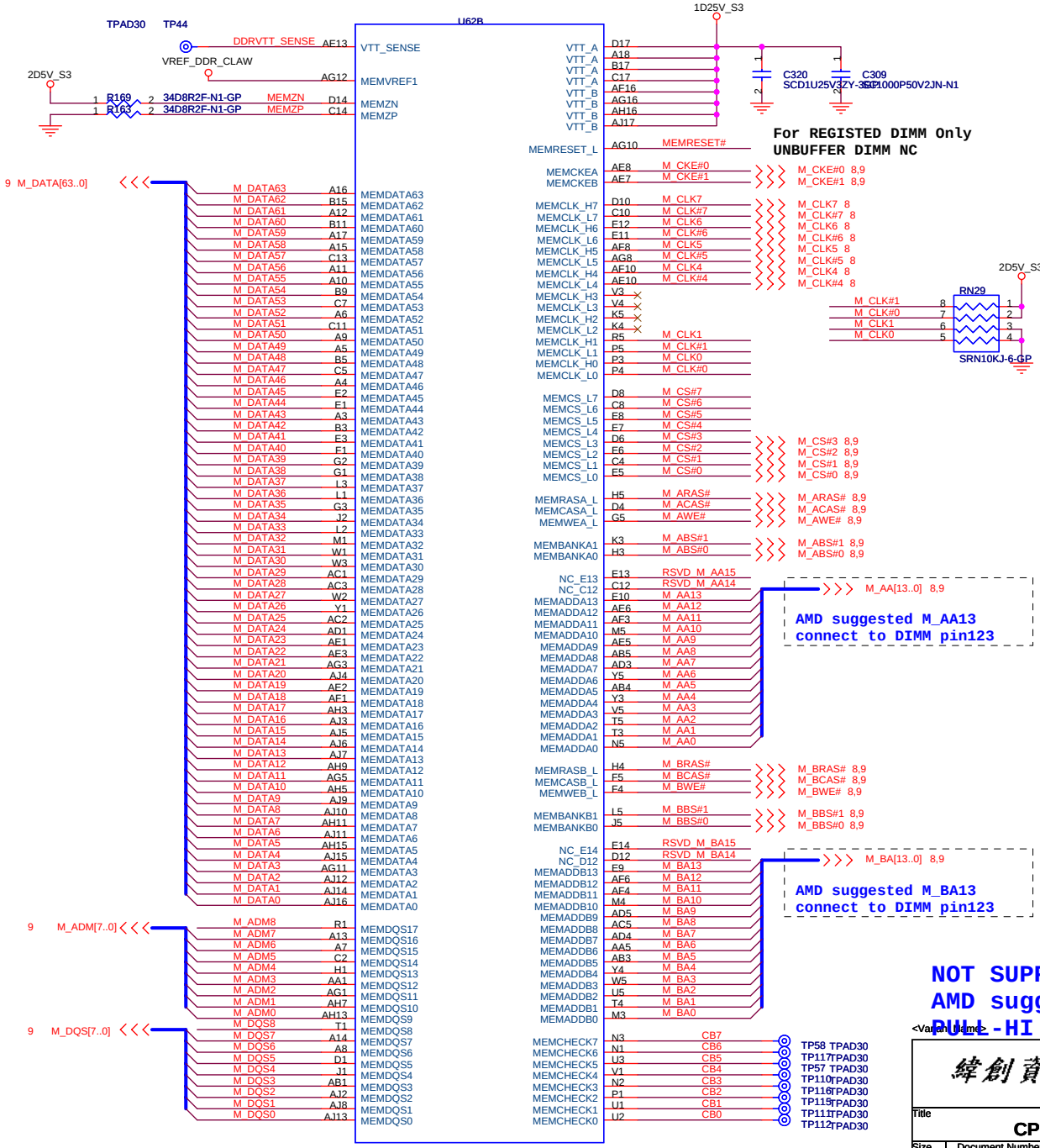
NOTE: Remove to bypass op-amp

VREF_DDR_CLAW



Place it near CPU



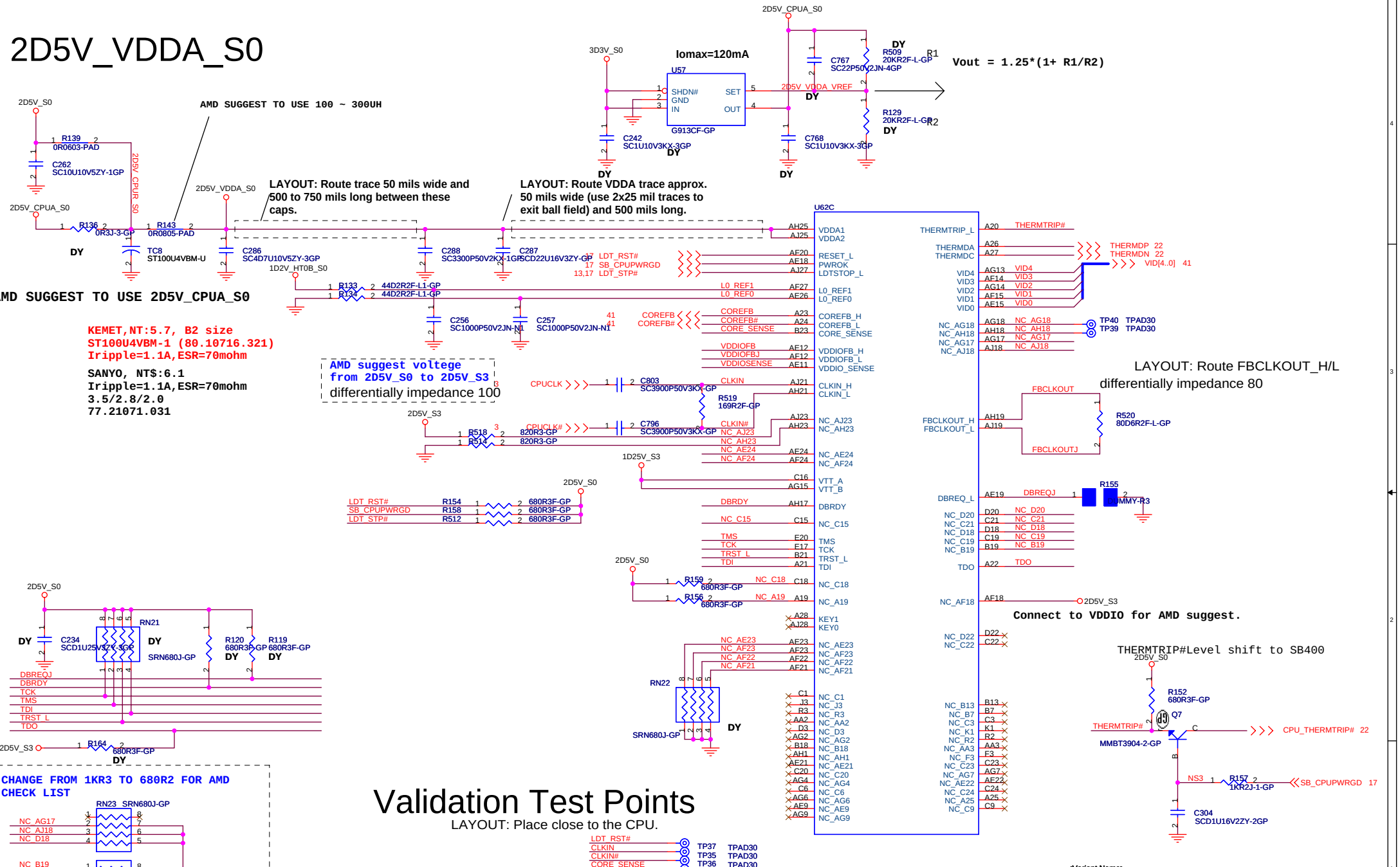


NOT SUPPORT ECC CHECK
AMD suggested remove
PULL-HI resistor.

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU(2/4)_DDR	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 5 of 58	

2D5V_VDDA_S0



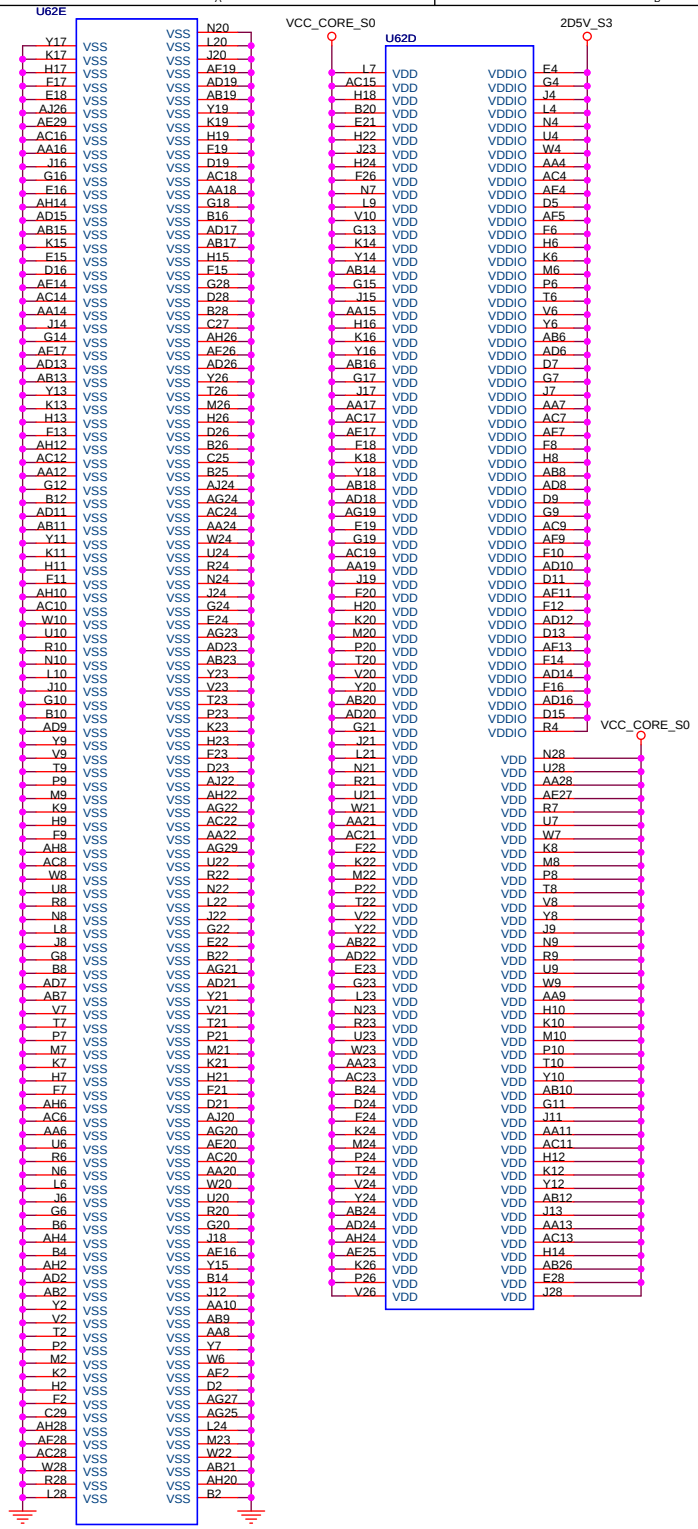
<Variant Name>

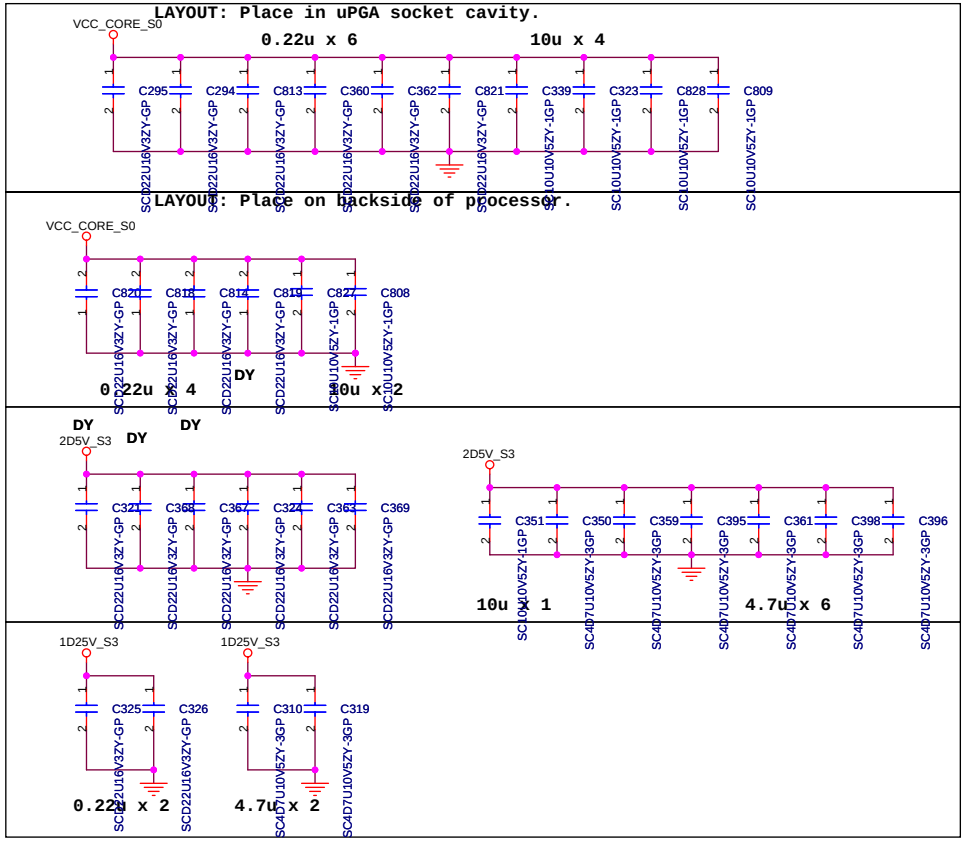
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(3/4)_Control & Debug

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 6 of 58





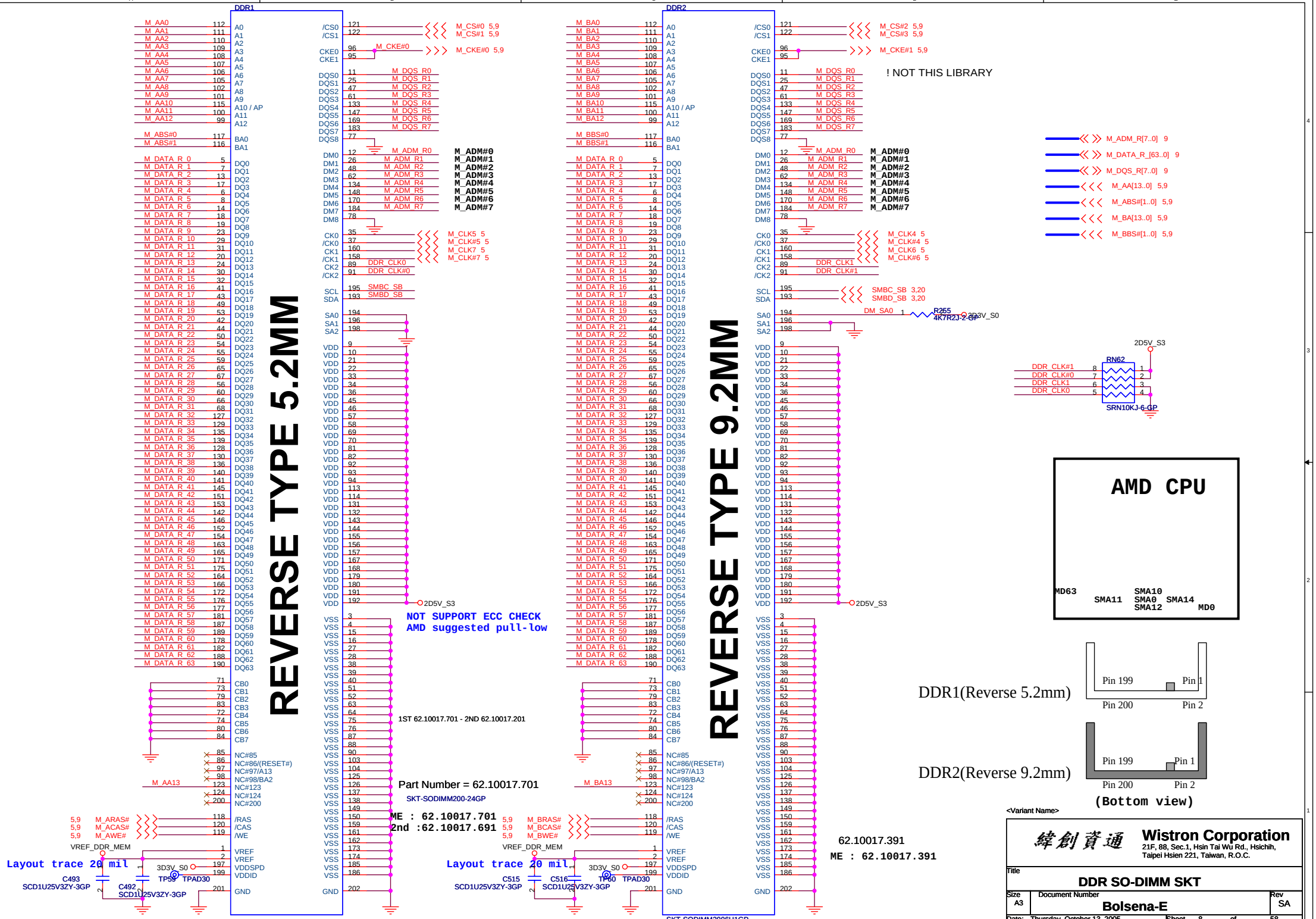
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(4/4)_Power

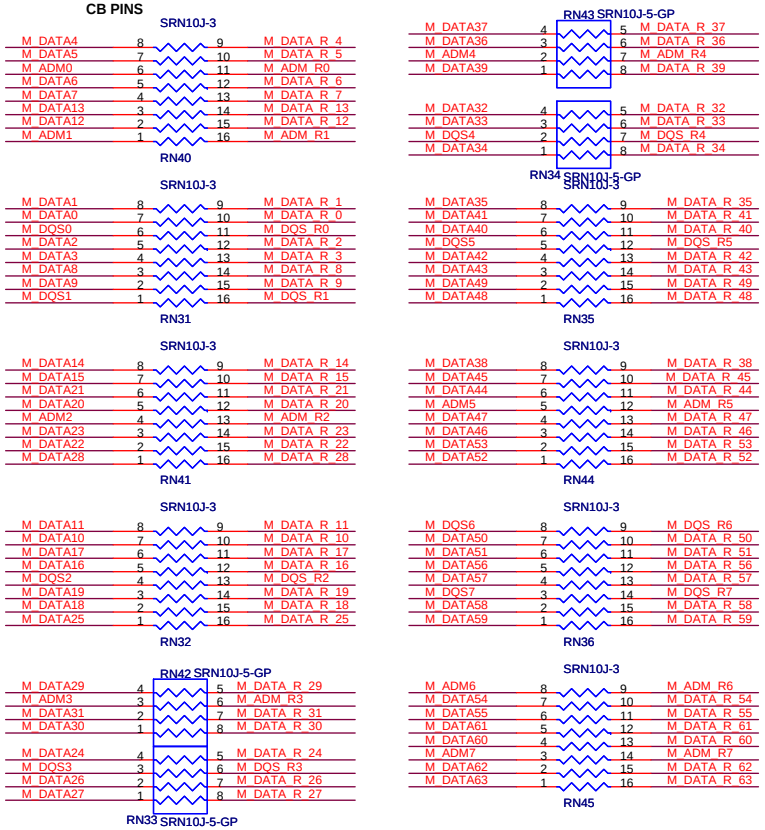
Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 7 of 58


DDR1
REVERSE TYPE 5.2MM
DDR2
REVERSE TYPE 9.2MM
! NOT THIS LIBRARY
NOT SUPPORT ECC CHECK
AMD suggested pull-low
1ST 62.10017.701 - 2ND 62.10017.201
Part Number = 62.10017.701
SKT-SODIMM200-24GP
ME : 62.10017.701
2nd :62.10017.691
62.10017.391
ME : 62.10017.391
SKT-SODIMM2006U1GP
Layout trace 20 mil
Layout trace 20 mil
M_ADM#0
M_ADM#1
M_ADM#2
M_ADM#3
M_ADM#4
M_ADM#5
M_ADM#6
M_ADM#7
M_ADM_R[7..0] 9
M_DATA_R_[63..0] 9
M_DQS_R[7..0] 9
M_AA[13..0] 5,9
M_ABS#[1..0] 5,9
M_BA[13..0] 5,9
M_BBS#[1..0] 5,9
R255
4K7R2J-2-GP
RN62
SRN10KJ-6-GP
AMD CPU
MD63
SMA11
SMA10
SMA0
SMA14
SMA12
MD0
DDR1(Reverse 5.2mm)
DDR2(Reverse 9.2mm)
Pin 199
Pin 1
Pin 200
Pin 2
(Bottom view)
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR SO-DIMM SKT
Size A3
Document Number
Bolsena-E
Rev SA
Date: Thursday, October 13, 2005
Sheet 8 of 58

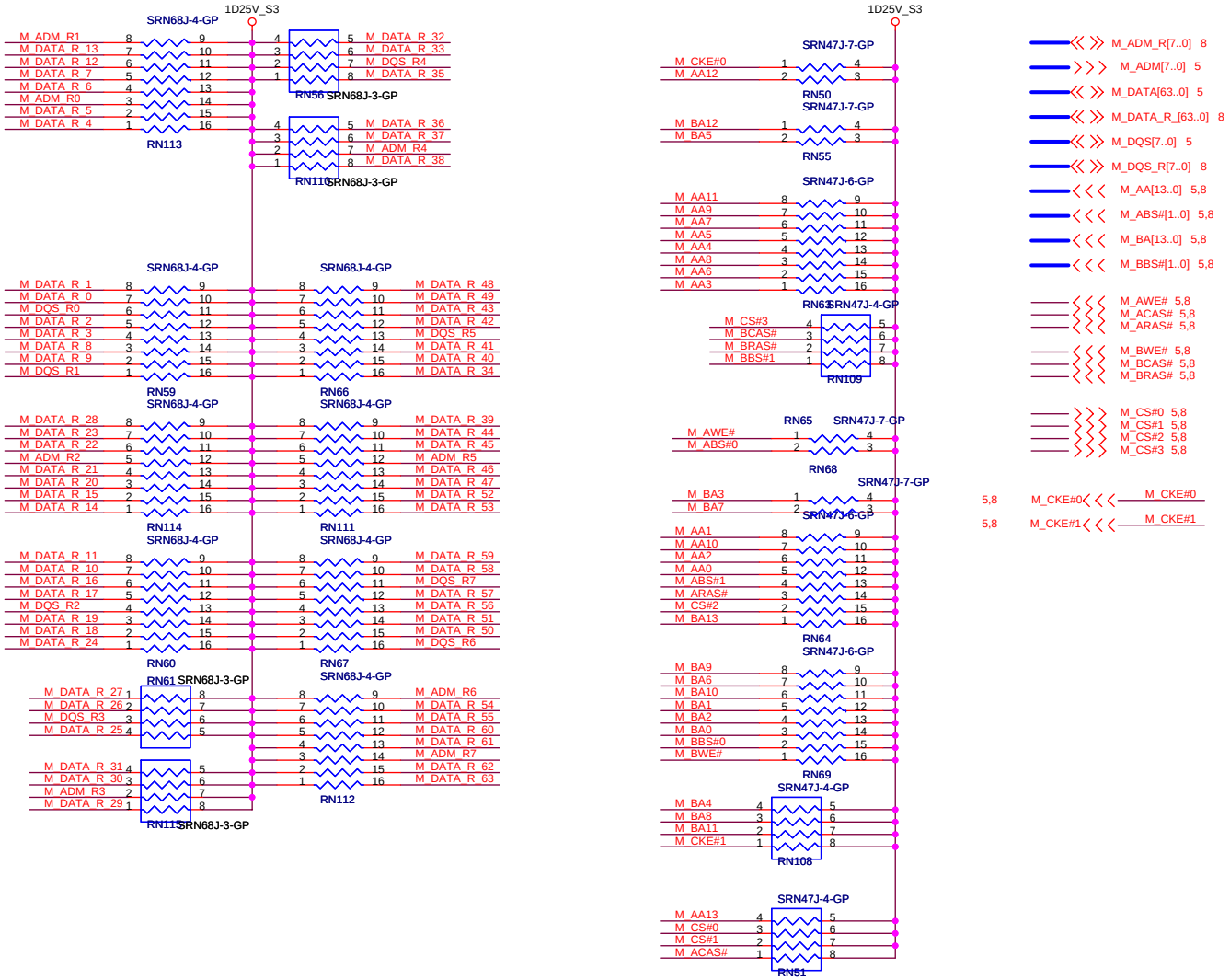
SERIES DAMPING

PLACE RNs CLOSE TO FIRST DIMM, < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS, CB PINS



PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION



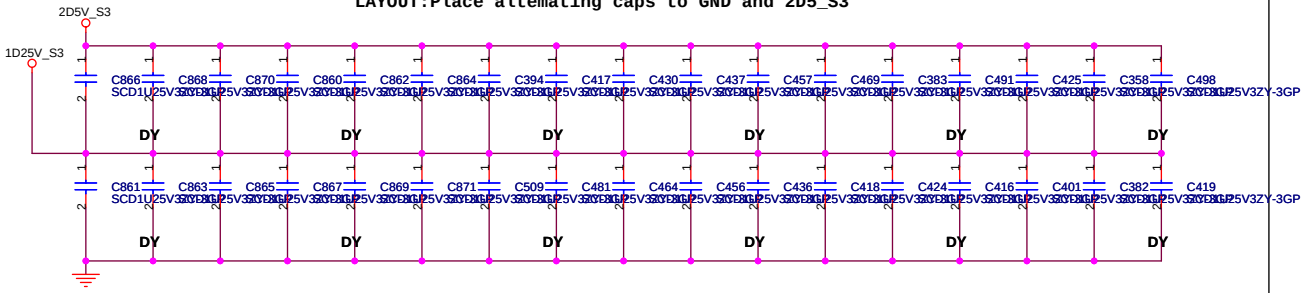
05/10
Remove the damping resistor for AMD suggest.

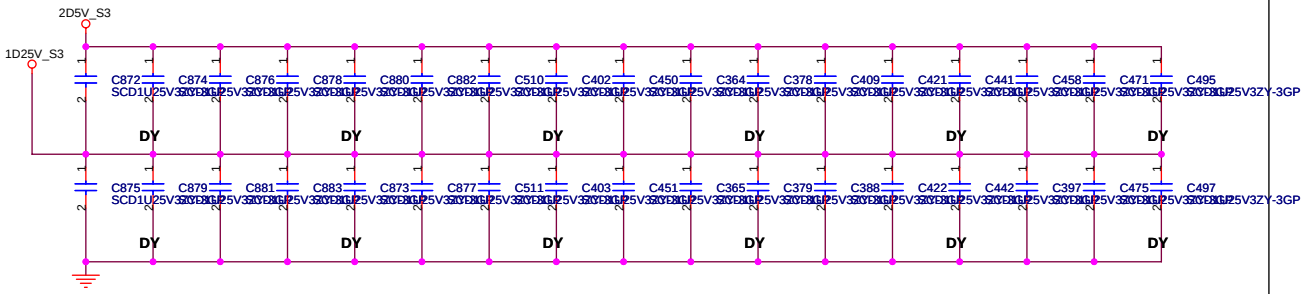
<Variant Name>

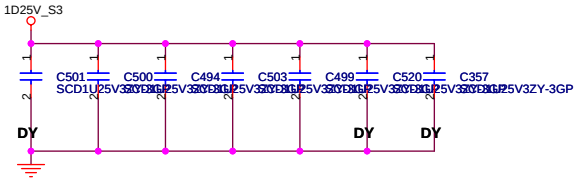
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR DAMPING & TERMINATION	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 9 of 58	

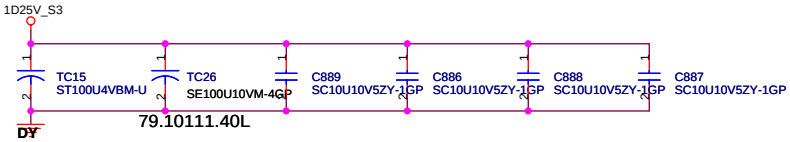
LAYOUT:Place altemating caps to GND and 2D5_S3



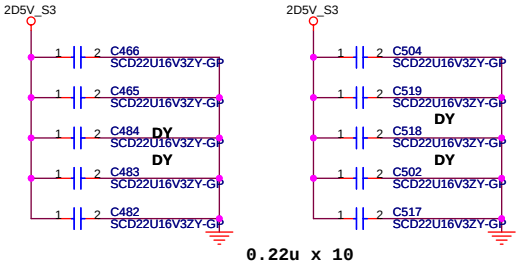




LAYOUT:Place at end of the DIMMs



LAYOUT:Place close to Power Pin of DDR socket.



0.22u x 10

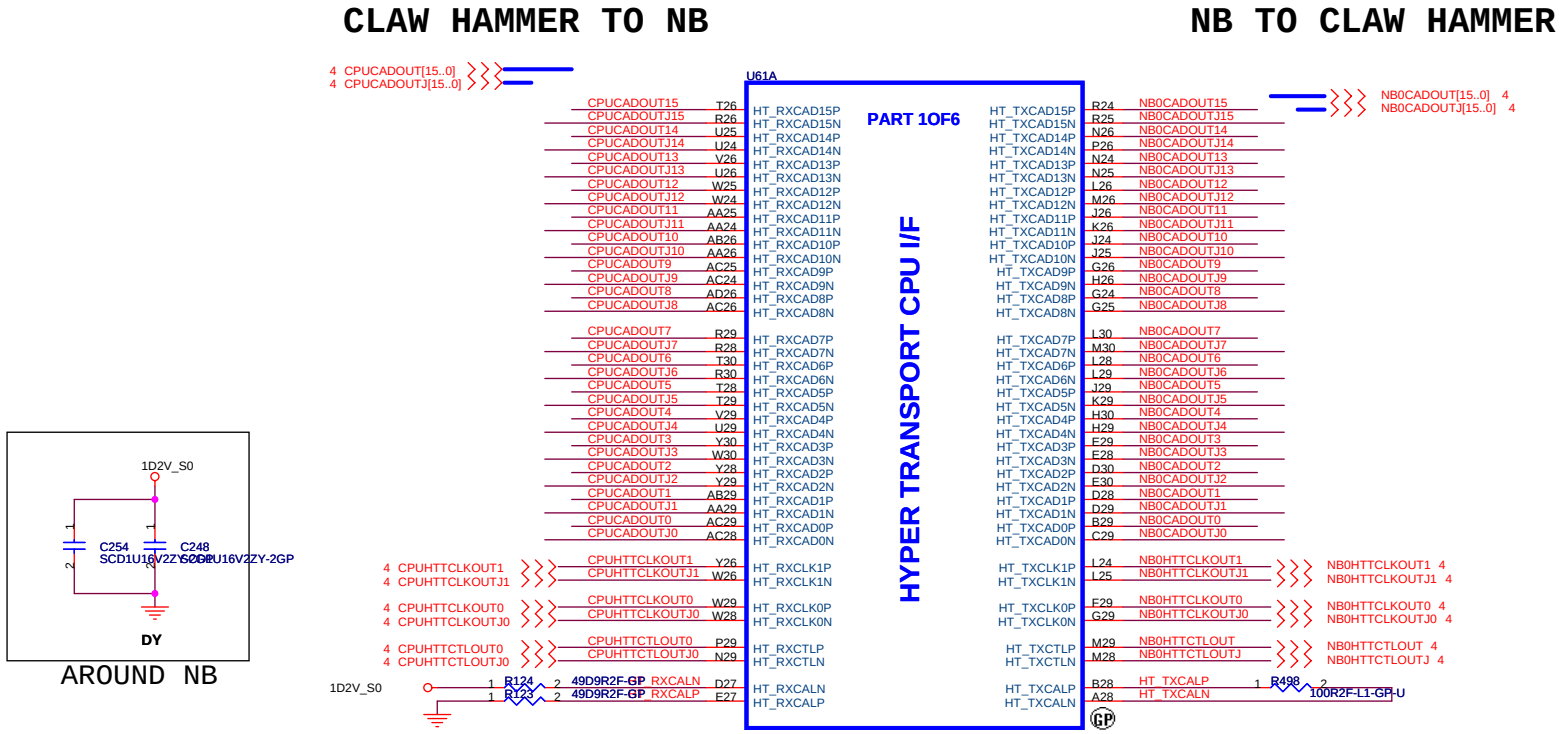
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR DECOUPLING

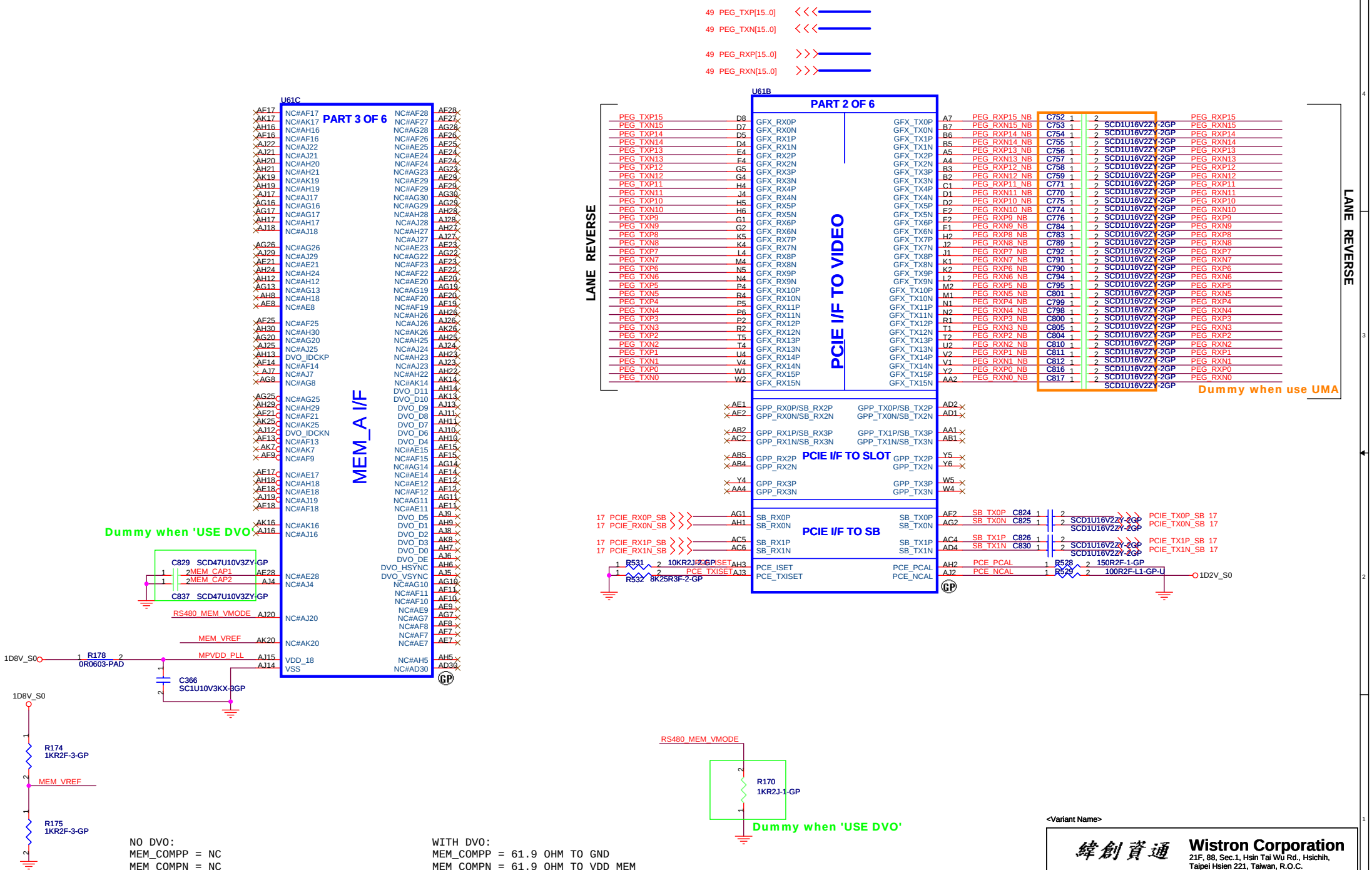
Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 10 of 58



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**ATI-RS482M (1 of 4) HT**	
Size A3	Document Number **Bolsena-E**	Rev SA
Date: Thursday, October 13, 2005	Sheet 11 of 58	



NO DVO:
MEM_COMPP = NC
MEM_COMPN = NC
MEM_CAP1 = 470nF
MEM_CAP2 = 470nF
MEM_VMODE = GND (IF VDD_MEM = 2.5V)
MEM_VREF = VDD_MEM / 2

WITH DVO:
MEM_COMPP = 61.9 OHM TO GND
MEM_COMPN = 61.9 OHM TO VDD_MEM
MEM_CAP1 = NC
MEM_CAP2 = NC
MEM_VMODE = 1.8V(IF VDD_MEM = 1.8V)
MEM_VREF = VDD_MEM / 2

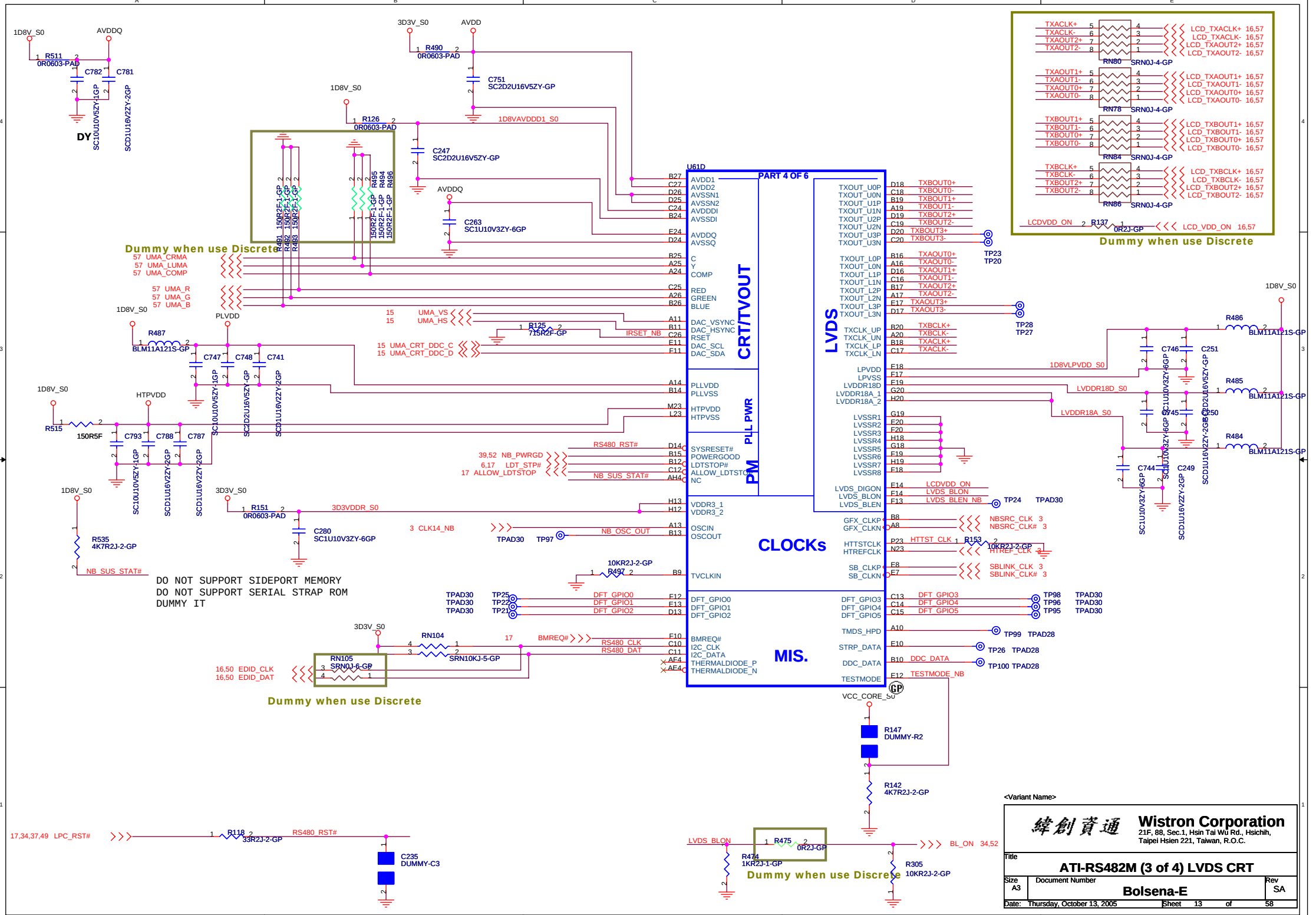
<Variant Name>

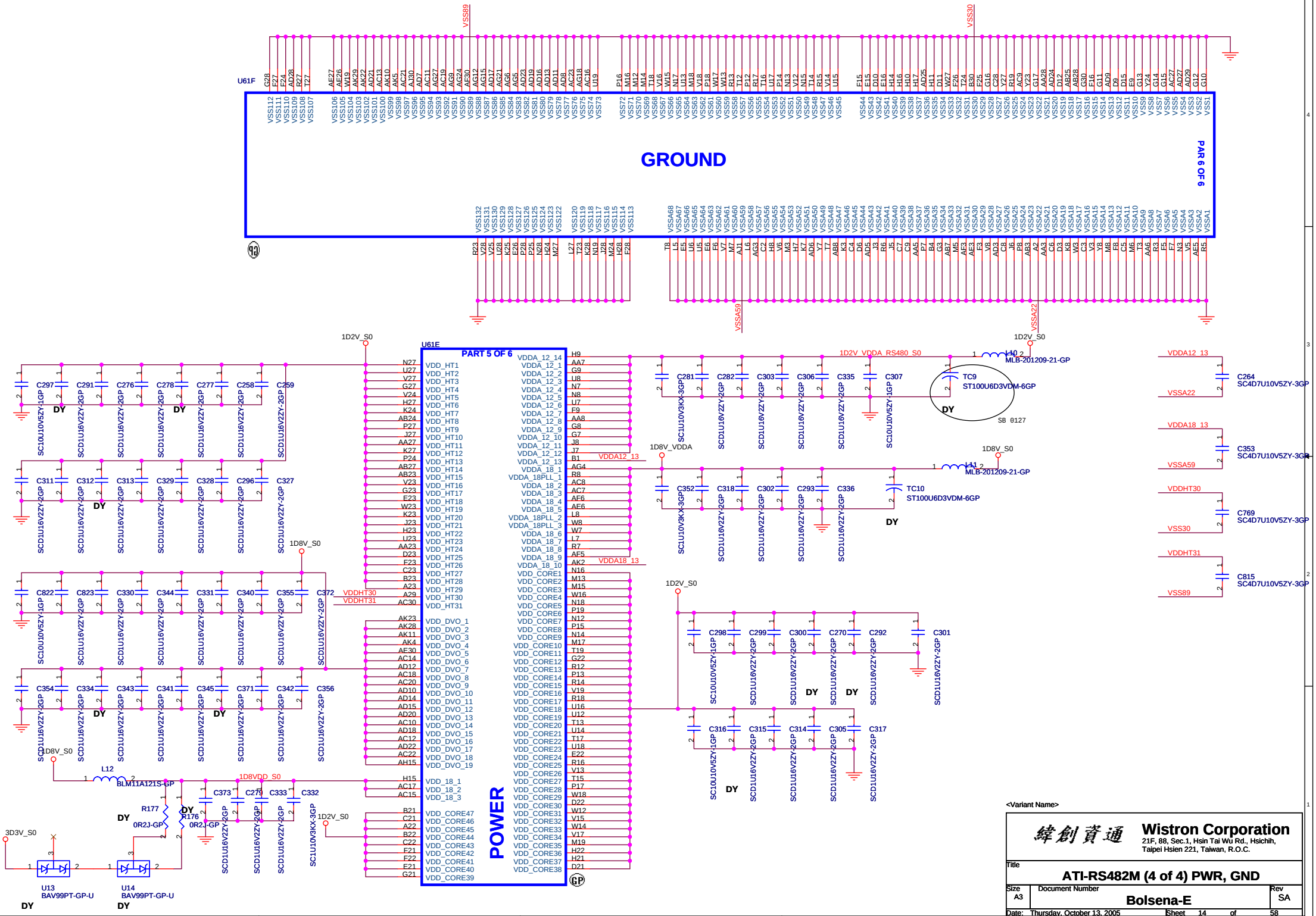
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-RS482M (2 of 4) PCIE**

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 12 of 58


U61D
PART 4 OF 6
CRT/TVOUT
LVDS
PLL PWR
PM
CLOCKs
MIS.
Dummy when use Discrete
DO NOT SUPPORT SIDEPORT MEMORY
DO NOT SUPPORT SERIAL STRAP ROM
DUMMY IT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-RS482M (3 of 4) LVDS CRT
Size A3
Document Number
Bolsena-E
Rev SA
Date: Thursday, October 13, 2005
Sheet 13 of 58



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

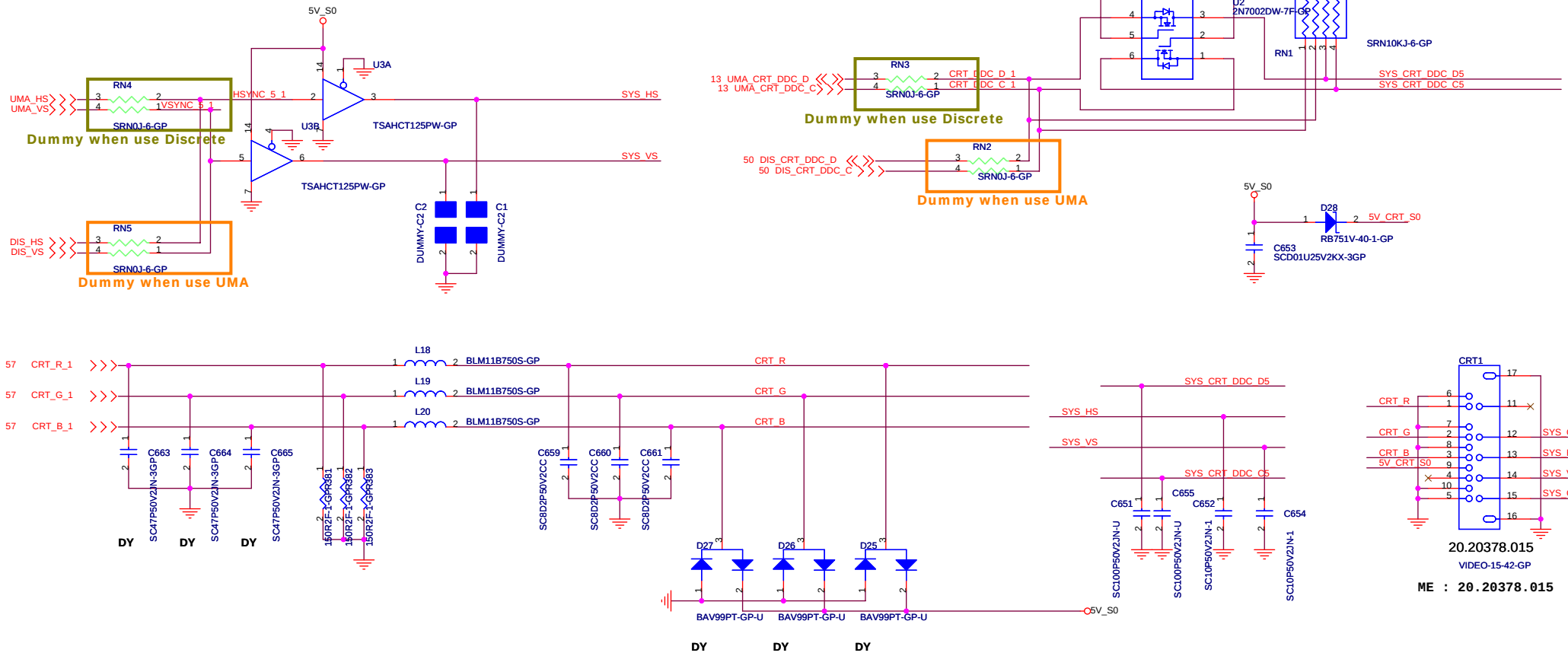
Title: ATI-RS482M (4 of 4) PWR, GND

Size: A3 | Document Number: Bolsena-E | Rev: SA

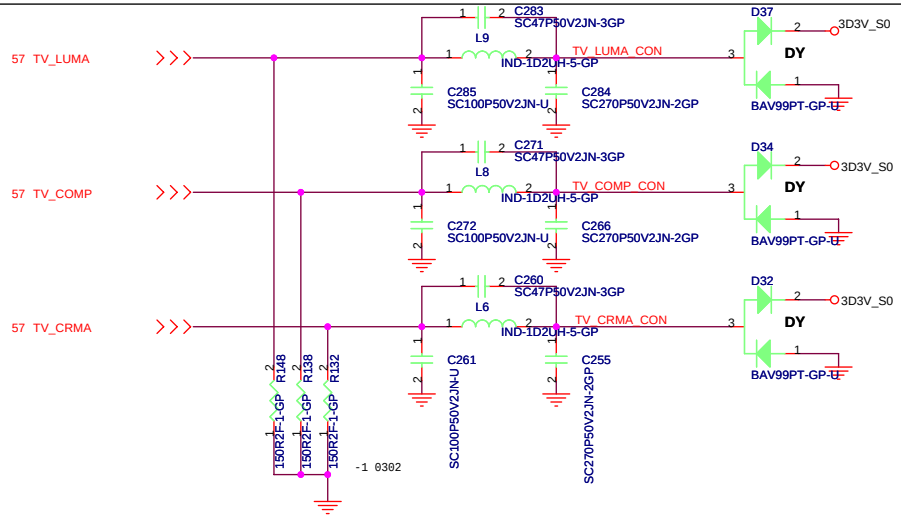
Date: Thursday, October 13, 2005 | Sheet 14 of 58

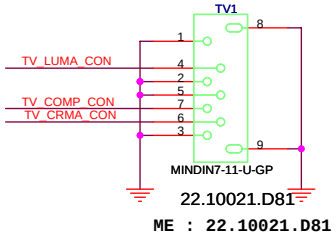
CRT CONN

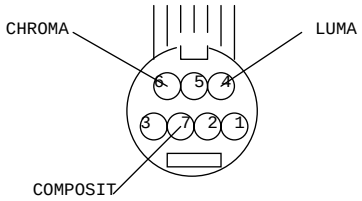
200mA Rating/Spec 500mA



TV CONN



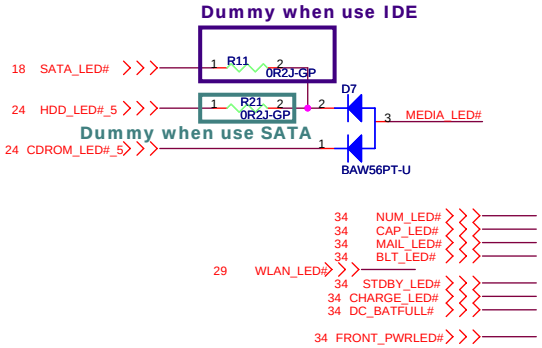


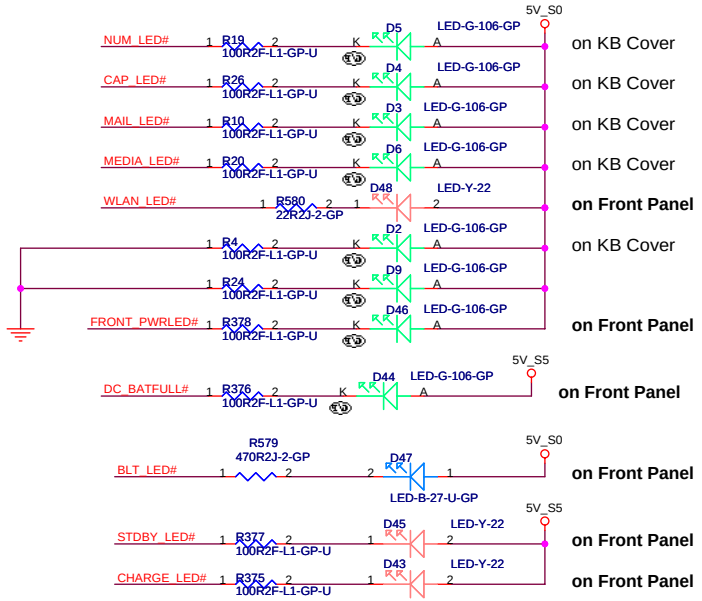


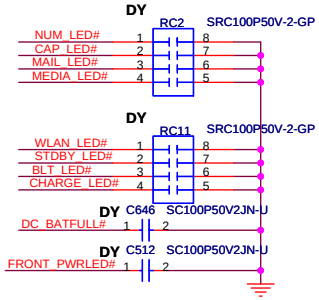
<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CRT/TV	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 15 of 58	

LEDs







on KB cover

-2 0408

LED	V	V				V	V	V
Button	V	V	V	V	V			
	POWER1	E-MAIL	INTERNET	e-BTN	PROGRAM	CAPS	NUM	HDD

Front panel

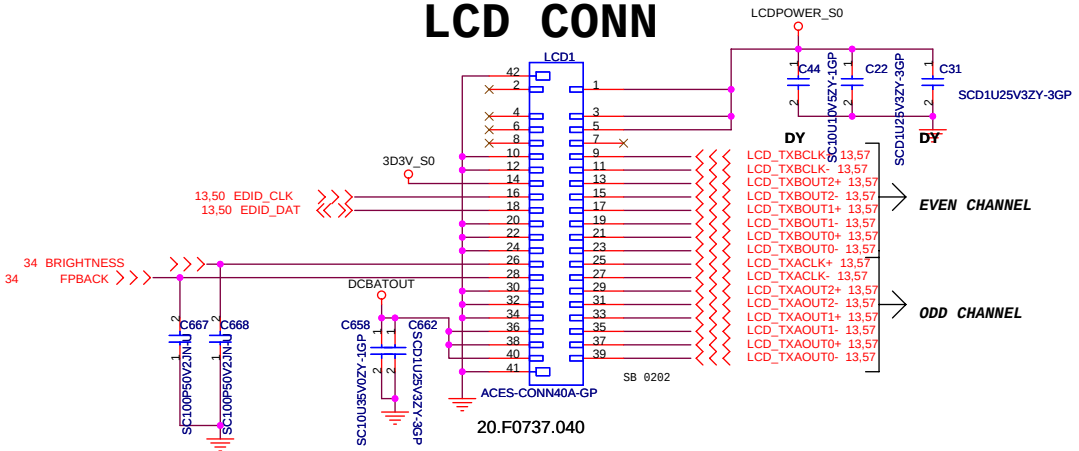
LED	V	V	V	V
Button	V	V		
	BlutTooth	Wireless	Charger	Power2

Charger:
Green : DC only with Battery full with DC
Orange : Charging
Orange Blink : Battery low

Power2:
Green : S0
Orange : S3
Orange Blinking : Enter S4

(Please See M.E. drawing LED position)

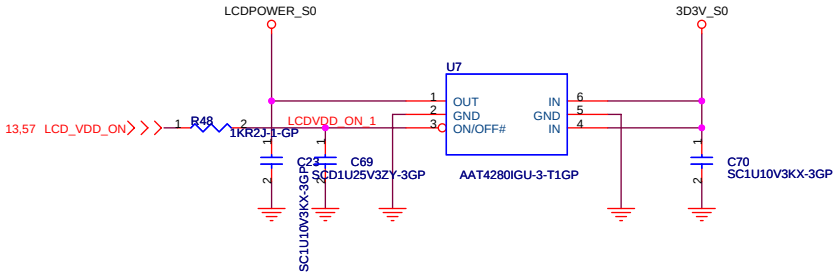
LCD CONN



1ST 20.D0198.108 - 2ND 20.F0687.040

LCD POWER

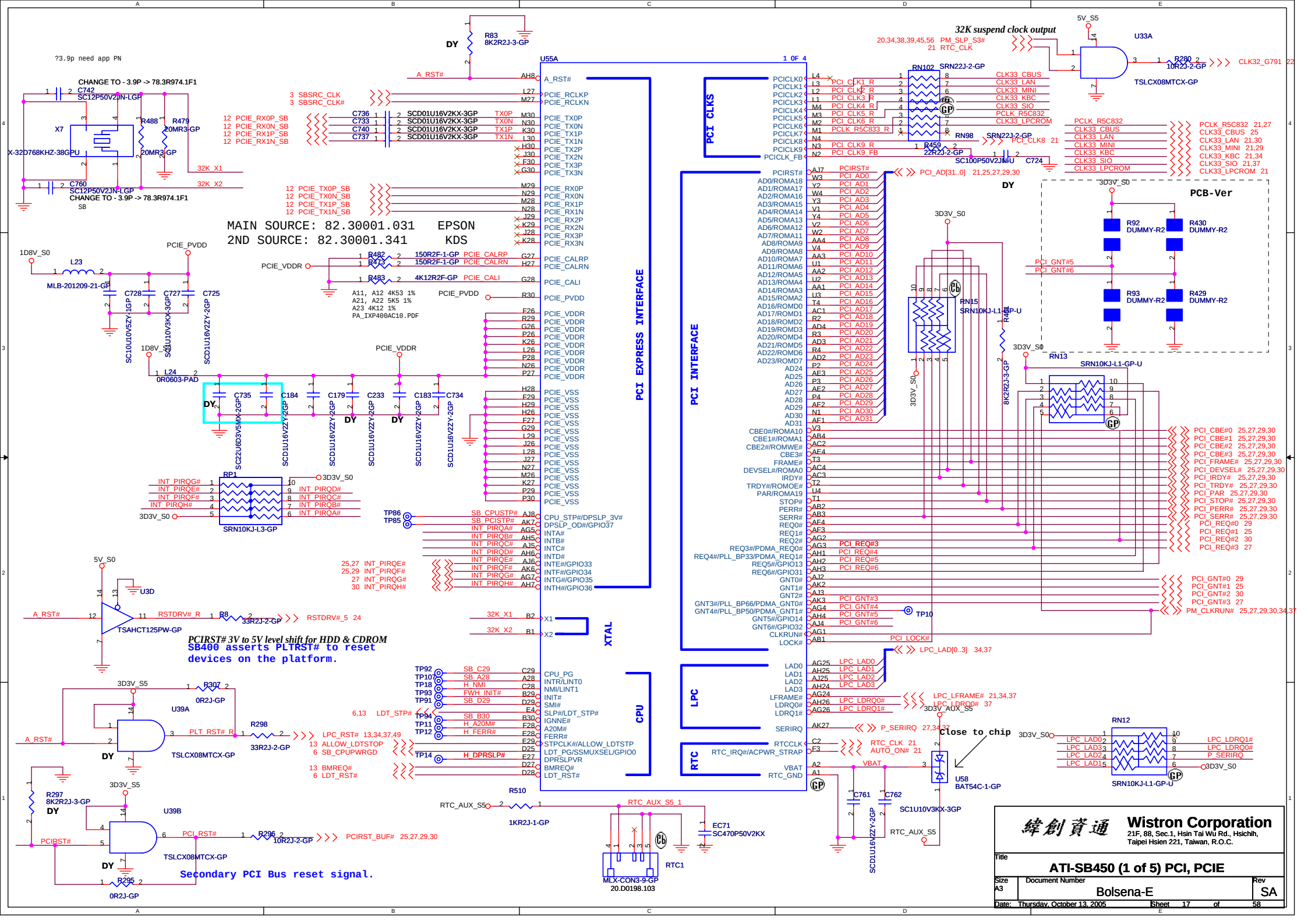
Layout 40 mil

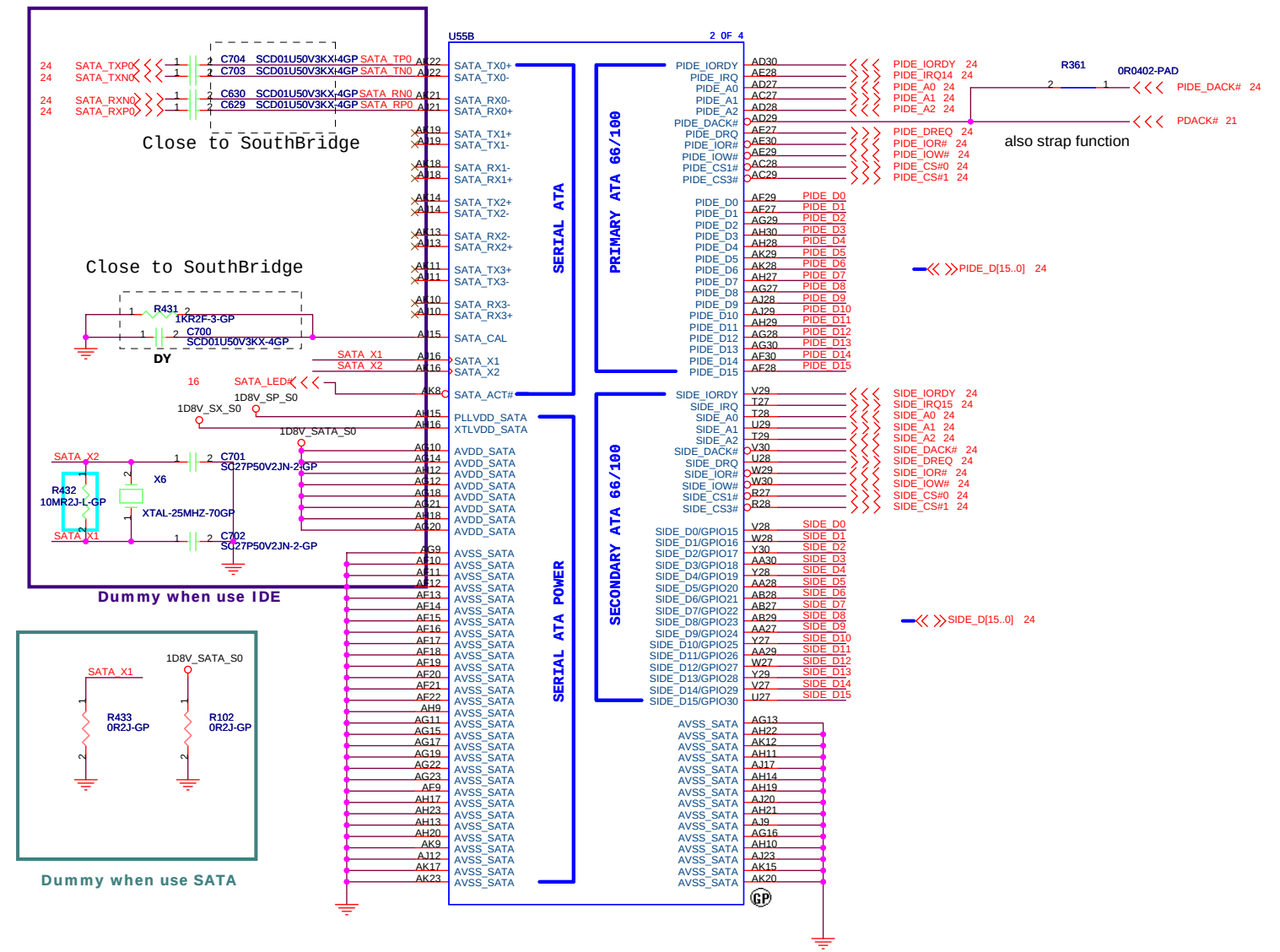


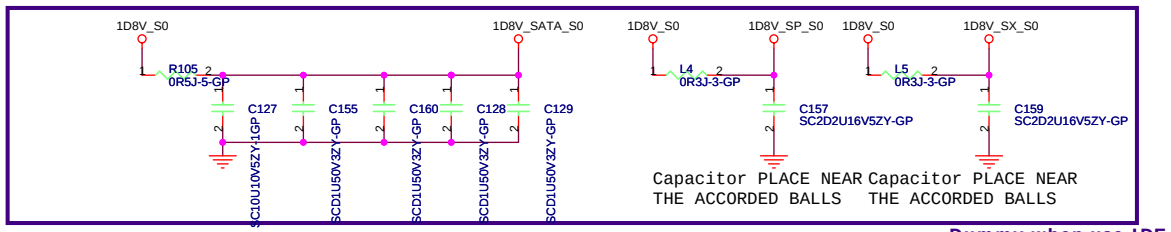
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD / LEDs	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 16 of 58	


MAIN SOURCE: 82.30001.031 EPSON
2ND SOURCE: 82.30001.341 KDS
U55A
1 0F 4
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
CPU
LPC
RTC
32K suspend clock output
PCIRST# 3V to 5V level shift for HDD & CDROM
SB400 asserts PLTRST# to reset devices on the platform.
Secondary PCI Bus reset signal.
Close to chip
PCB-Ver
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-SB450 (1 of 5) PCI, PCIE
Size A3
Document Number
Bolsena-E
Rev SA
Date: Thursday, October 13, 2005
Sheet 17 of 58





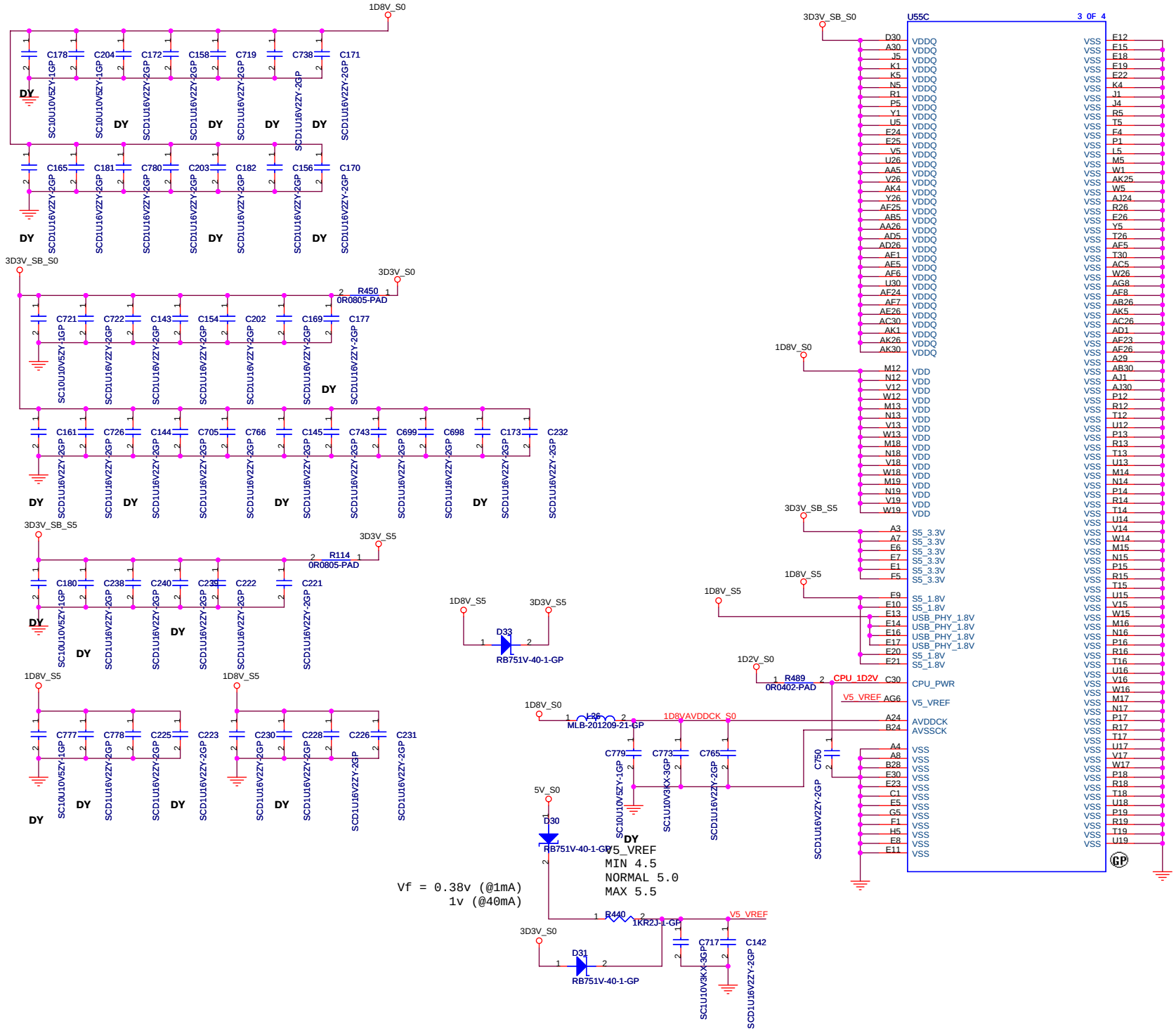
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB400 (2 of 5) IDE**

Size: A3 | Document Number: **Bolsena-E** | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 18 of 58



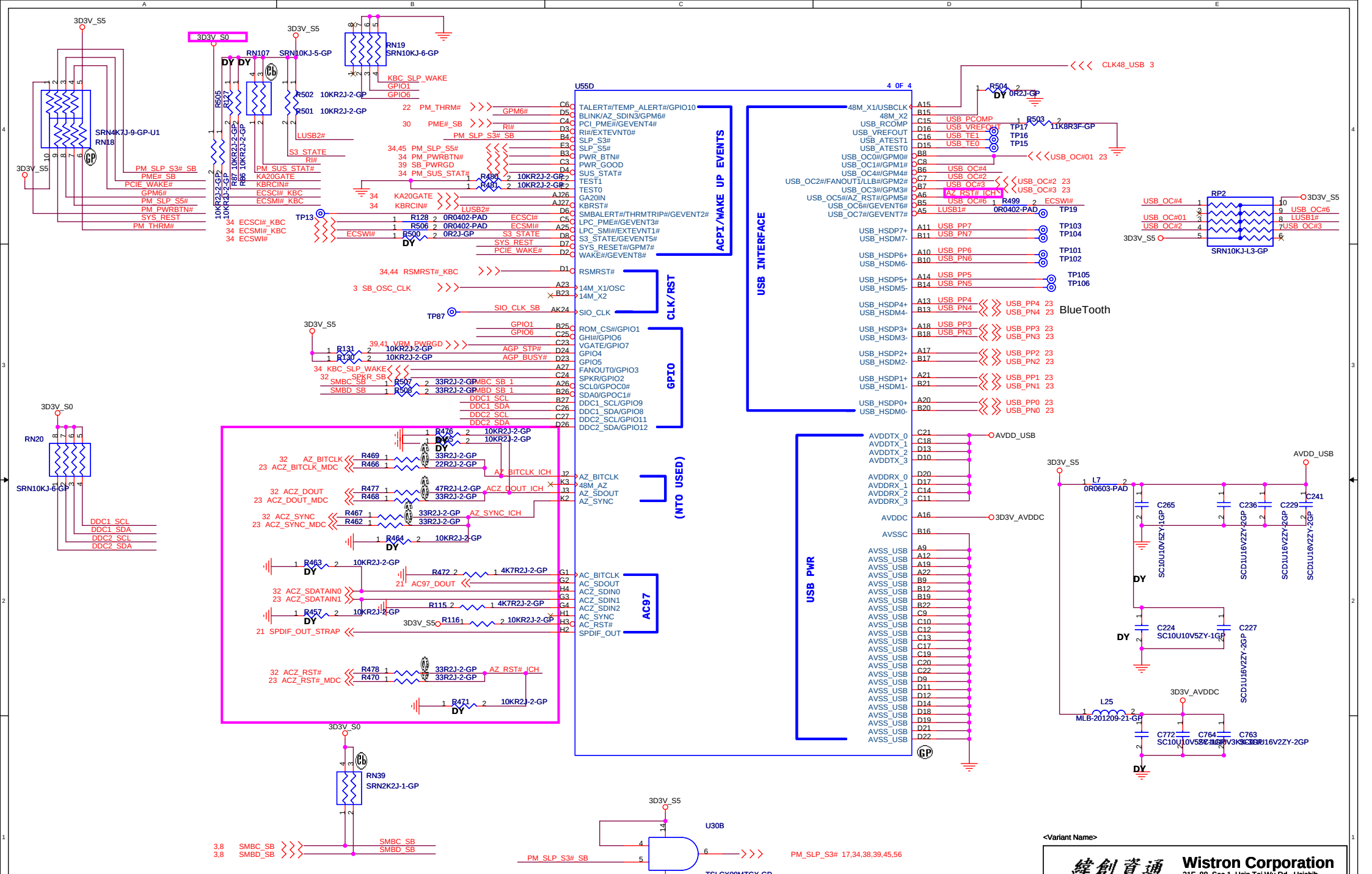
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 (3 of 5) POWER

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 19 of 58



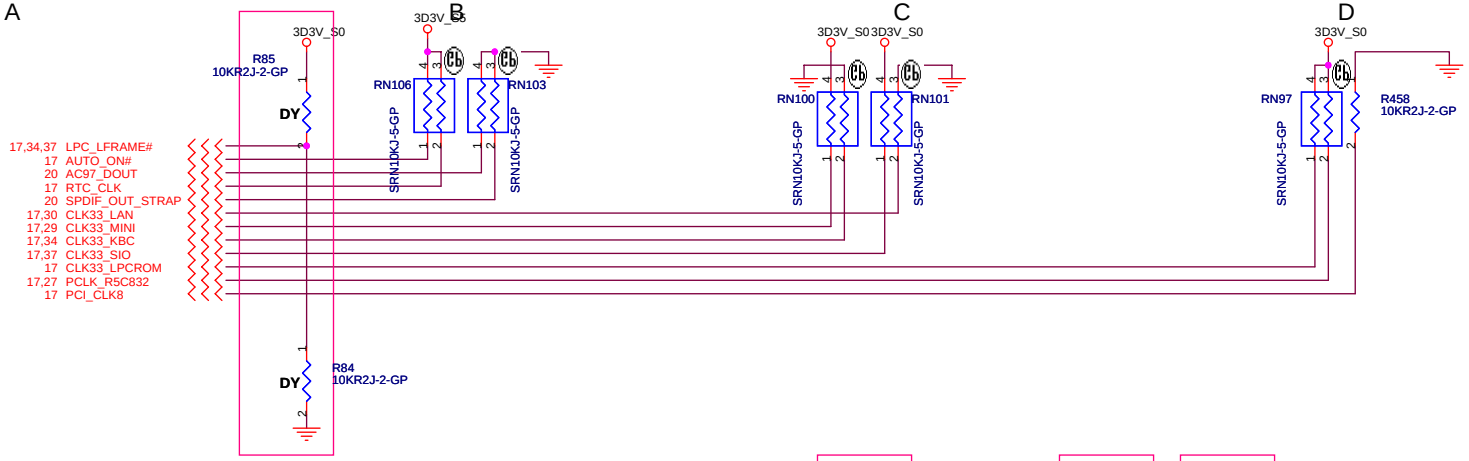
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: ATI-SB450 (4 of 5) USB GPIO

Size: A3 | Document Number: Bolsena-E | Rev: SA

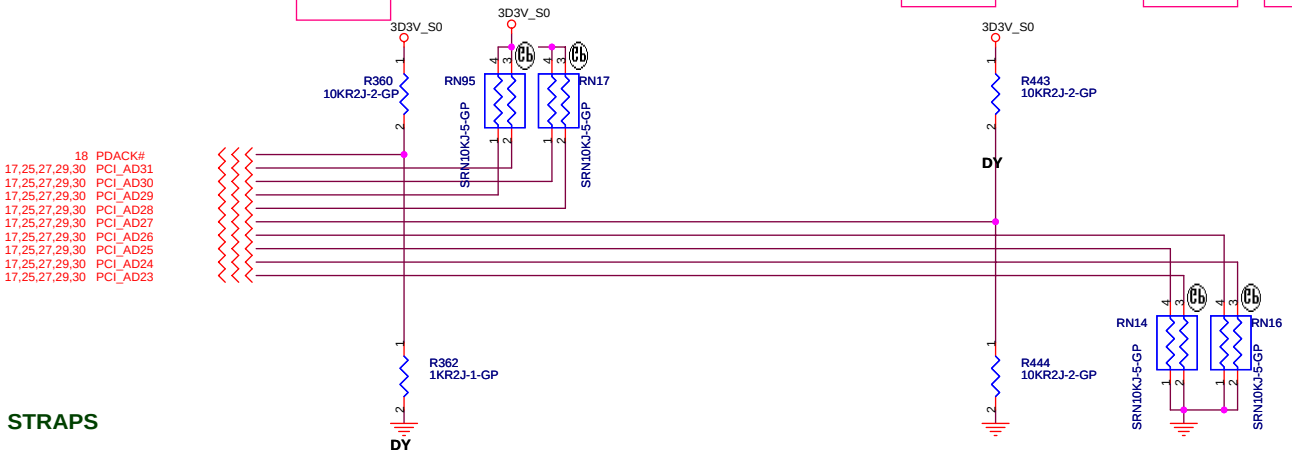
Date: Thursday, October 13, 2005 | Sheet 20 of 58



Place these R close to SouthBridge if possible

REQUIRED SYSTEM STRAPS

	LFRAME#	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2 (CLK33_LAN)	PCI_CLK3 (CLK33_MINI)	PCI_CLK4 (CLK33_KBC)	PCI_CLK5 (CLK33_SIO)	PCI_CLK6 (CLK33_LPCROM)	PCI_CLK7 (PCLK_R5C832) PCI_CLK8
STRAP HIGH	Thermal Trip is not enable as default Optional	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHZ -Crytsal Pad	USB PHY PWRDOWN DISABLE DEFAULT	USB INT PLL48	PCIE_CM_SET HIGH DEFAULT	CPU I/F=K8 DEFAULT	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I
STRAP LOW	Thermal Trip is enable as default Optional	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTENNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz DEFAULT	48MHZ-Clock Input Buffer DEFAULT	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ Use External only	PCIE_CM_SET LOW	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

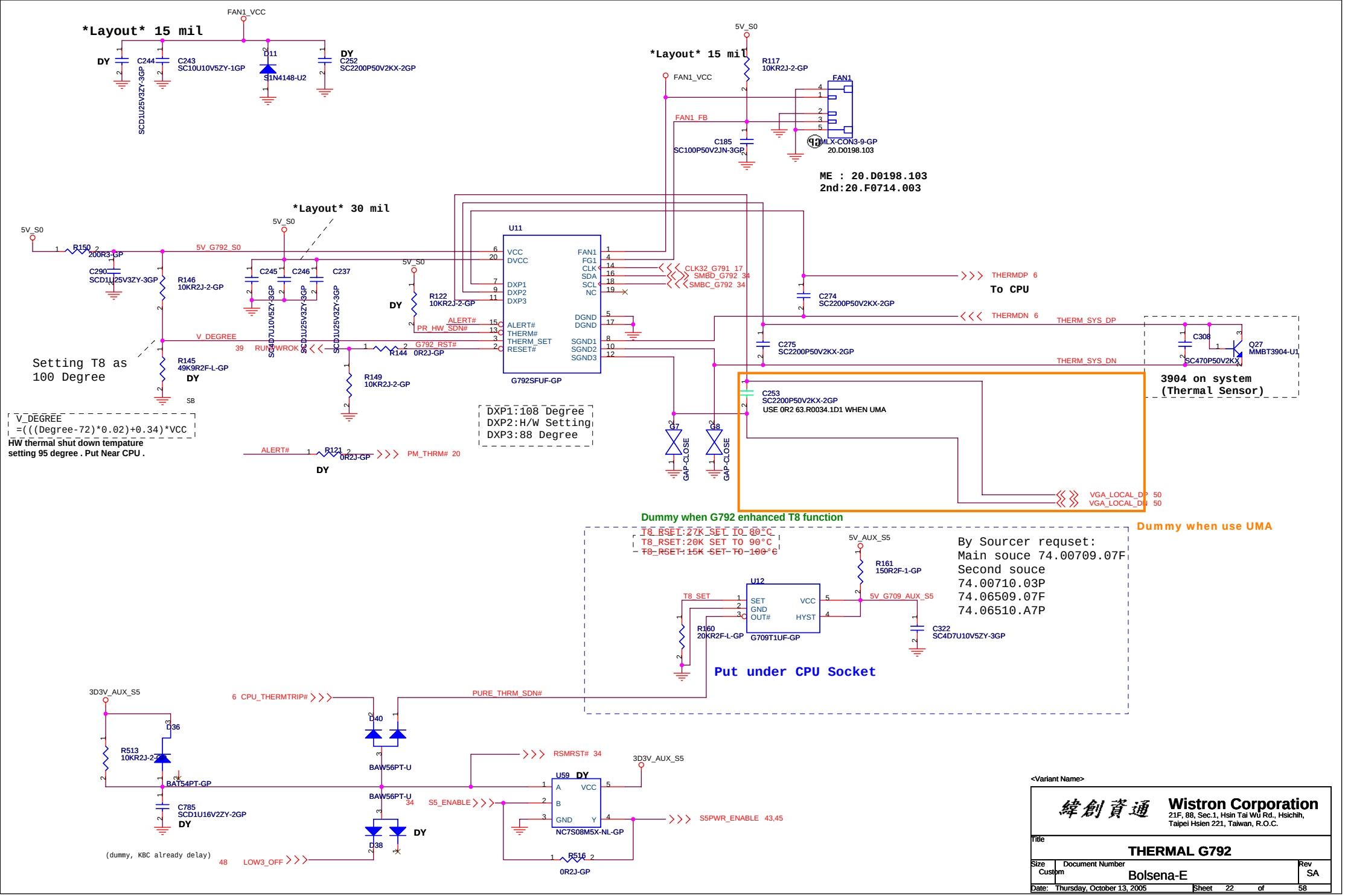
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 STRAPPING(5 of 5)

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 21 of 58


Layout 15 mil
FAN1_VCC
DY
C244
SCD1U25V3ZY-3GP
C243
SC10U10V5ZY-1GP
D11
S1N4148-U2
DY
C252
SC2200P50V2KX-2GP
Layout 15 mil
5V_S0
R117
10KR2J-2-GP
FAN1_VCC
FAN1
FAN1_FB
C185
SC100P50V2JN-3GP
MLX-CON3-9-GP
20.D0198.103
ME : 20.D0198.103
2nd:20.F0714.003
Layout 30 mil
5V_S0
R150
200R3-GP
5V_G792_S0
C290
SCD1U25V3ZY-3GP
R146
10KR2J-2-GP
C245
C246
C237
SCD7U10V5ZY-3GP
SCD1U25V3ZY-3GP
SCD1U25V3ZY-3GP
5V_S0
DY
R122
10KR2J-2-GP
U11
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC
DGND
DGND
SGND1
SGND2
SGND3
CLK32_G791 17
SMBD_G792 34
SMBC_G792 34
THERMDP 6
To CPU
C274
SC2200P50V2KX-2GP
THERMDN 6
THERM_SYS_DP
THERM_SYS_DN
C308
SC470P50V2KX
Q27
MMBT3904-U1
3904 on system
(Thermal Sensor)
ALERT#
PR_HW_SDN#
V_DEGREE
39 RUN_PWROK
R144
0R2J-GP
G792_RST#
R149
10KR2J-2-GP
G792SFUF-GP
Setting T8 as
100 Degree
R145
49K9R2F-L-GP
DY
SB
C275
SC2200P50V2KX-2GP
C253
SC2200P50V2KX-2GP
USE 0R2 63.R0034.1D1 WHEN UMA
G7
G8
GAP-CLOSE
GAP-CLOSE
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
HW thermal shut down tempature
setting 95 degree . Put Near CPU .
ALERT#
R121
0R2J-GP
PM_THRM# 20
DY
VGA_LOCAL_DP 50
VGA_LOCAL_DN 50
Dummy when G792 enhanced T8 function
Dummy when use UMA
T8_RSET:27K SET TO 80°C
T8_RSET:20K SET TO 90°C
T8_RSET:15K SET TO 100°C
5V_AUX_S5
R161
150R2F-1-GP
U12
SET
GND
OUT#
VCC
HYST
T8_SET
5V_G709_AUX_S5
R160
20KR2F-L-GP
G709T1UF-GP
C322
SC4D7U10V5ZY-3GP
By Sourcer requset:
Main souce 74.00709.07F
Second souce
74.00710.03P
74.06509.07F
74.06510.A7P
Put under CPU Socket
3D3V_AUX_S5
6 CPU_THERMTRIP#
PURE_THRM_SDN#
D36
R513
10KR2J-2-GP
BAT54PT-GP
C785
SCD1U16V2ZY-2GP
DY
D40
BAW56PT-U
BAW56PT-U
34
D38
DY
RSMRST# 34
3D3V_AUX_S5
U59
DY
A
B
GND
VCC
Y
NC7S08M5X-NL-GP
S5_ENABLE
S5PWR_ENABLE 43,45
R516
0R2J-GP
(dummy, KBC already delay)
48 LOW3_OFF
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
THERMAL G792
Size
Custom
Document Number
Bolsena-E
Rev
SA
Date: Thursday, October 13, 2005
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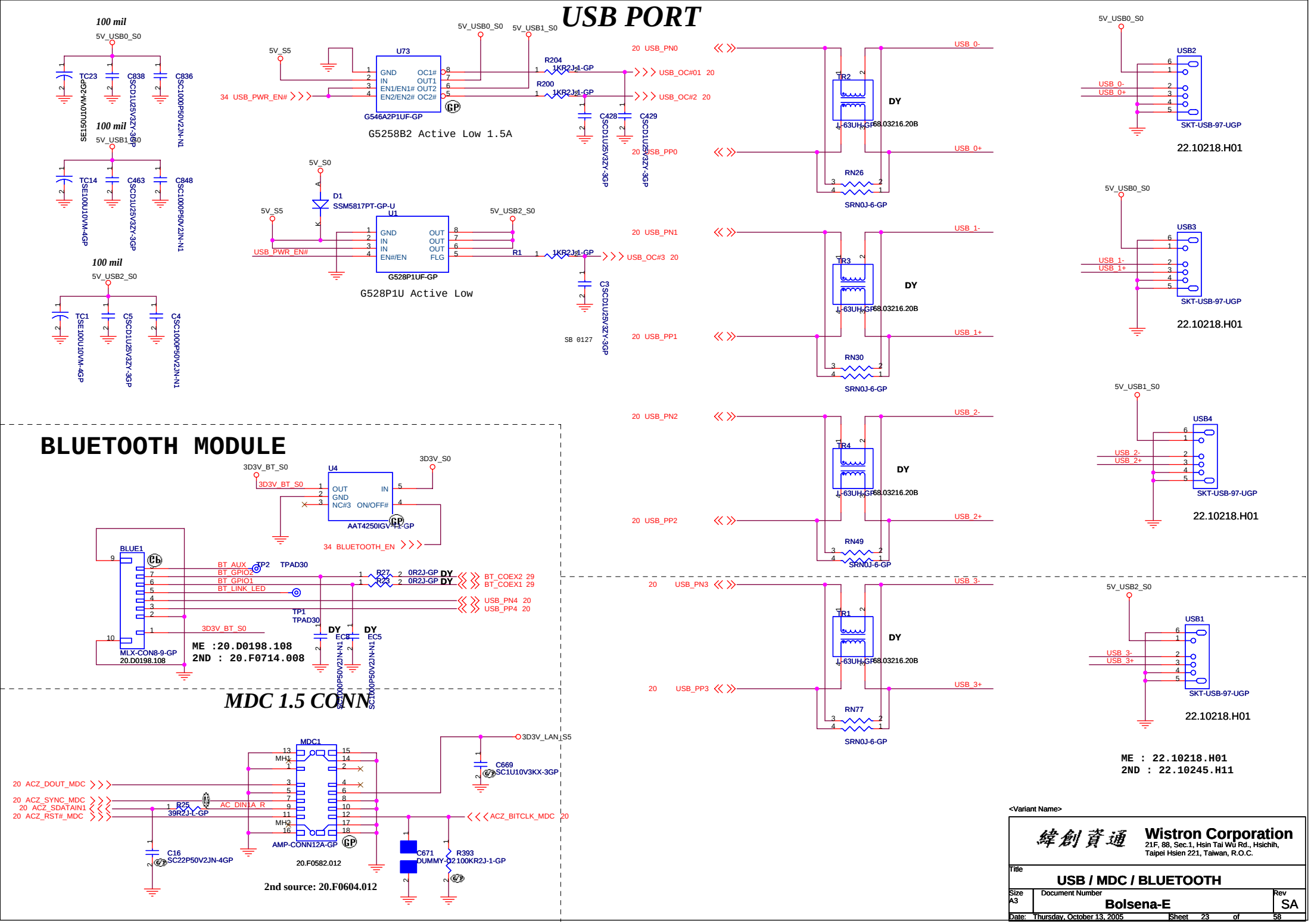
USB PORT



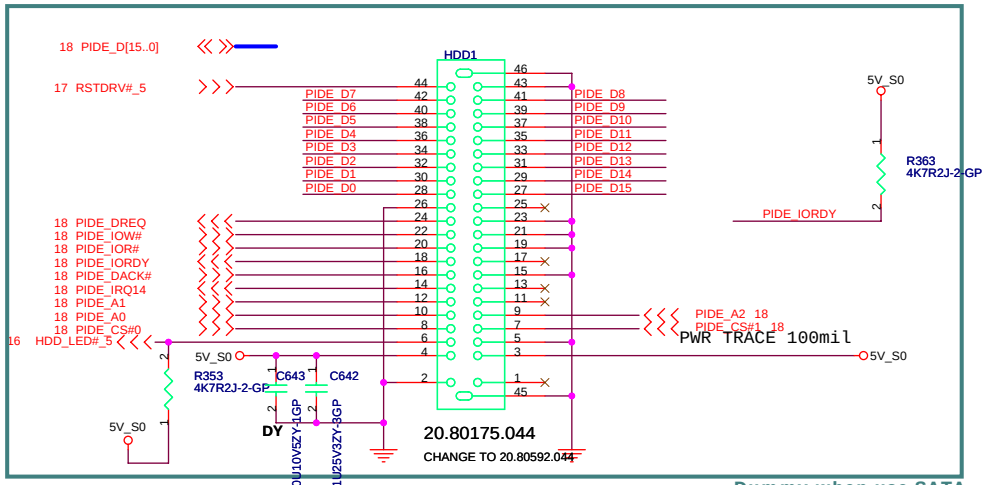
BLUETOOTH MODULE

MDC 1.5 CONN

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**USB / MDC / BLUETOOTH**	
Size A3	Document Number **Bolsena-E**	Rev SA
Date: Thursday, October 13, 2005	Sheet 23 of 58	

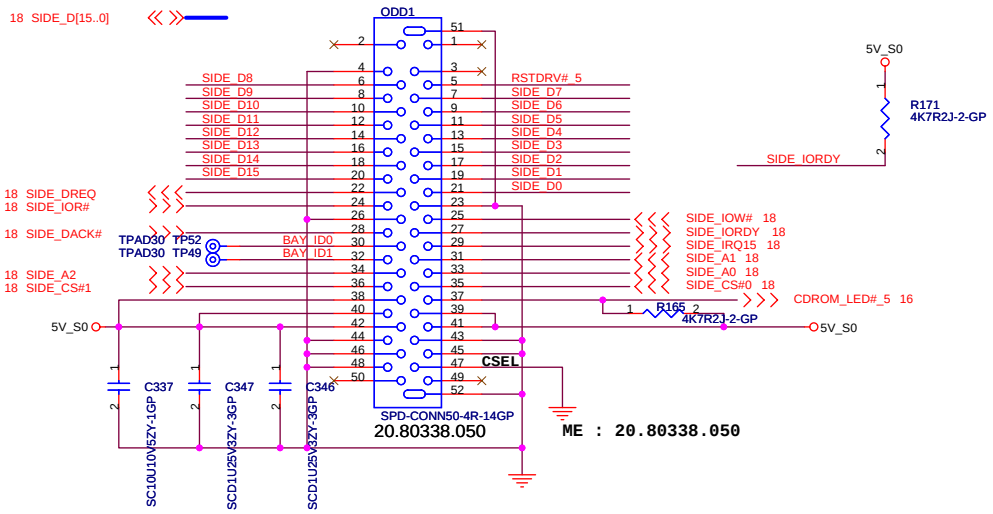
HDD



Dummy when use SATA

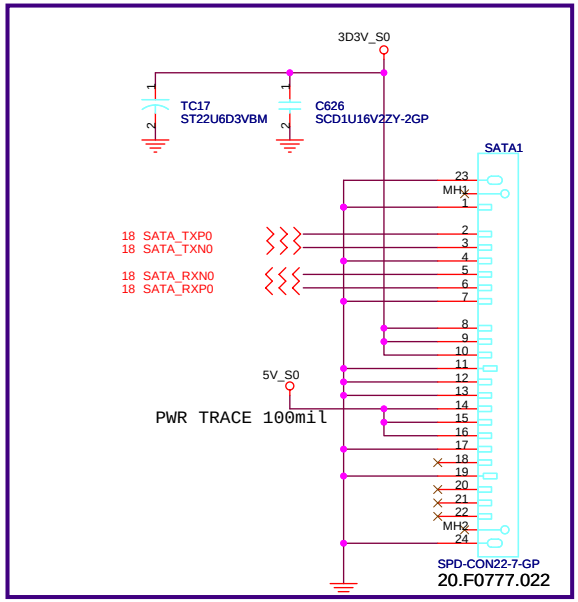
ME : 20.80592.044
(DIFFERENT FROM ORCAD P/N)

CDROM



ME : 20.80338.050

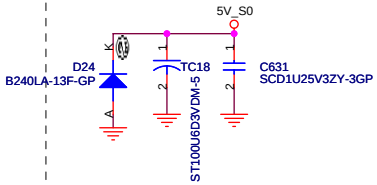
SATA Connector



Dummy when use IDE

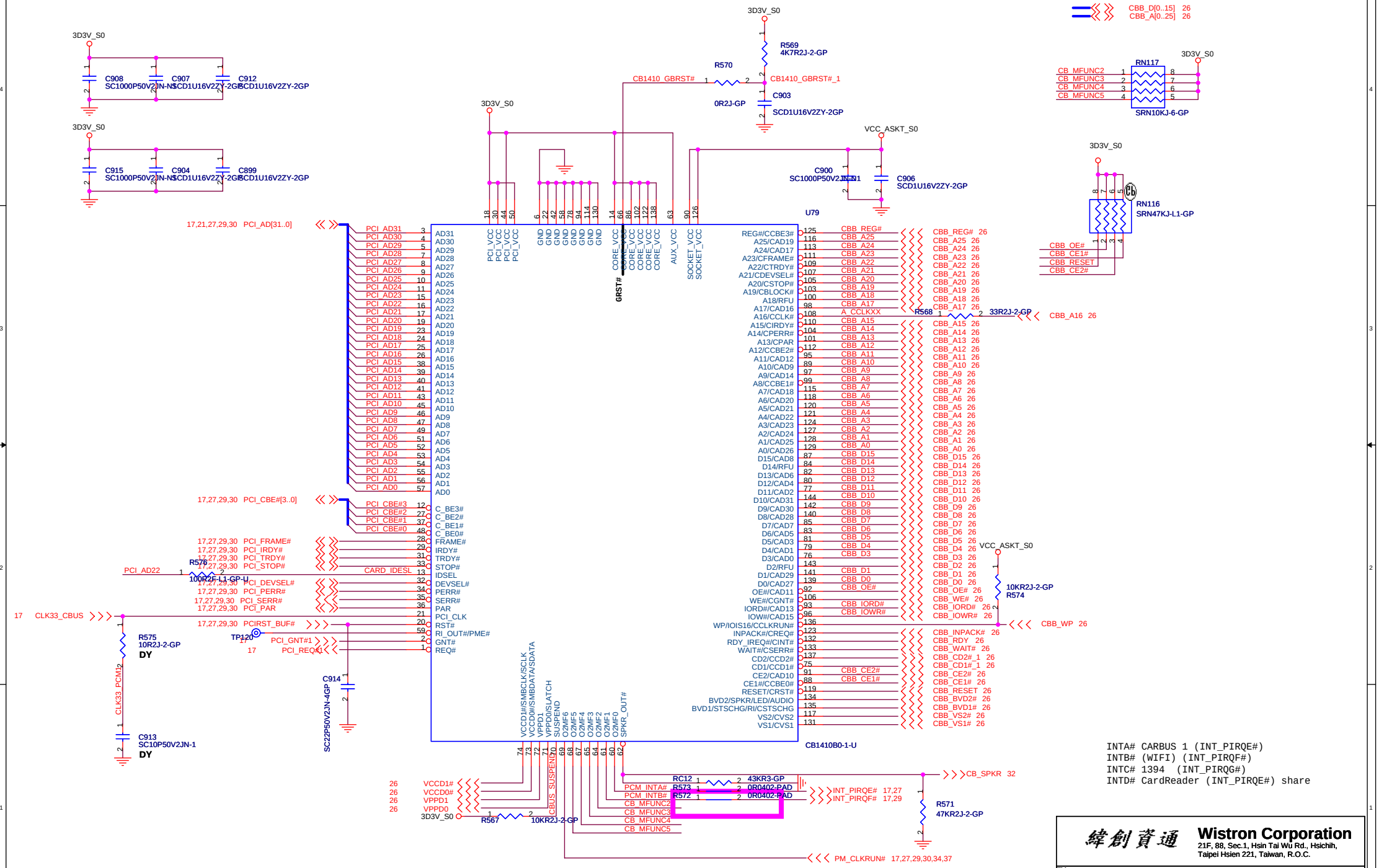
ME : 20.F0777.022

For HDD & SATA both



<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD / CDROM / SATA	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 24 of 58	


3D3V_S0
C908 SC1000P50V2JN-NS
C907 SCD1U16V2ZY-2GP
C912 SCD1U16V2ZY-2GP
C915 SC1000P50V2JN-NS
C904 SCD1U16V2ZY-2GP
C899 SCD1U16V2ZY-2GP
R569 4K7R2J-2-GP
R570 0R2J-GP
CB1410_GBRST#
CB1410_GBRST#_1
C903 SCD1U16V2ZY-2GP
VCC_ASKT_S0
C900 SC1000P50V2JN-N1
C906 SCD1U16V2ZY-2GP
CBB_D[0..15] 26
CBB_A[0..25] 26
RN117 SRN10KJ-6-GP
CB_MFUNC2
CB_MFUNC3
CB_MFUNC4
CB_MFUNC5
RN116 SRN47KJ-L1-GP
CBB_OE#
CBB_CE1#
CBB_RESET
CBB_CE2#
U79
17,21,27,29,30 PCI_AD[31..0]
17,27,29,30 PCI_CBE#[3..0]
17,27,29,30 PCI_FRAME#
17,27,29,30 PCI_IRDY#
17,27,29,30 PCI_TRDY#
17,27,29,30 PCI_STOP#
17,27,29,30 PCI_DEVSEL#
17,27,29,30 PCI_PERR#
17,27,29,30 PCI_SERR#
17,27,29,30 PCI_PAR
17,27,29,30 PCIRST_BUF#
PCI_GNT#1
PCI_REQ#1
PCI_AD22
R576 100R2F-L1-GP-U
CARD_IDESL
17 CLK33_CBUS
R575 10R2J-2-GP DY
TP120
CLK33_PCM12
C913 SC10P50V2JN-1 DY
C914 SC22P50V2JN-4GP
CB1410B0-1-U
R568 33R2J-2-GP
CBB_A16 26
R574 10KR2J-2-GP
CBB_WP 26
VCCD1#
VCCD0#
VPPD1
VPPD0
R567 10KR2J-2-GP
CBUS_SUSPEND
PCM_INTA#
PCM_INTB#
RC12 43KR3-GP
R573 0R0402-PAD
R572 0R0402-PAD
INT_PIRQE# 17,27
INT_PIRQF# 17,29
CB_SPKR 32
R571 47KR2J-2-GP
PM_CLKRUN# 17,27,29,30,34,37
INTA# CARBUS 1 (INT_PIRQE#)
INTB# (WIFI) (INT_PIRQF#)
INTC# 1394 (INT_PIRQG#)
INTD# CardReader (INT_PIRQE#) share
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CardBus_ENE CB1410
Size A3
Document Number
Bolsena-E
Rev SA
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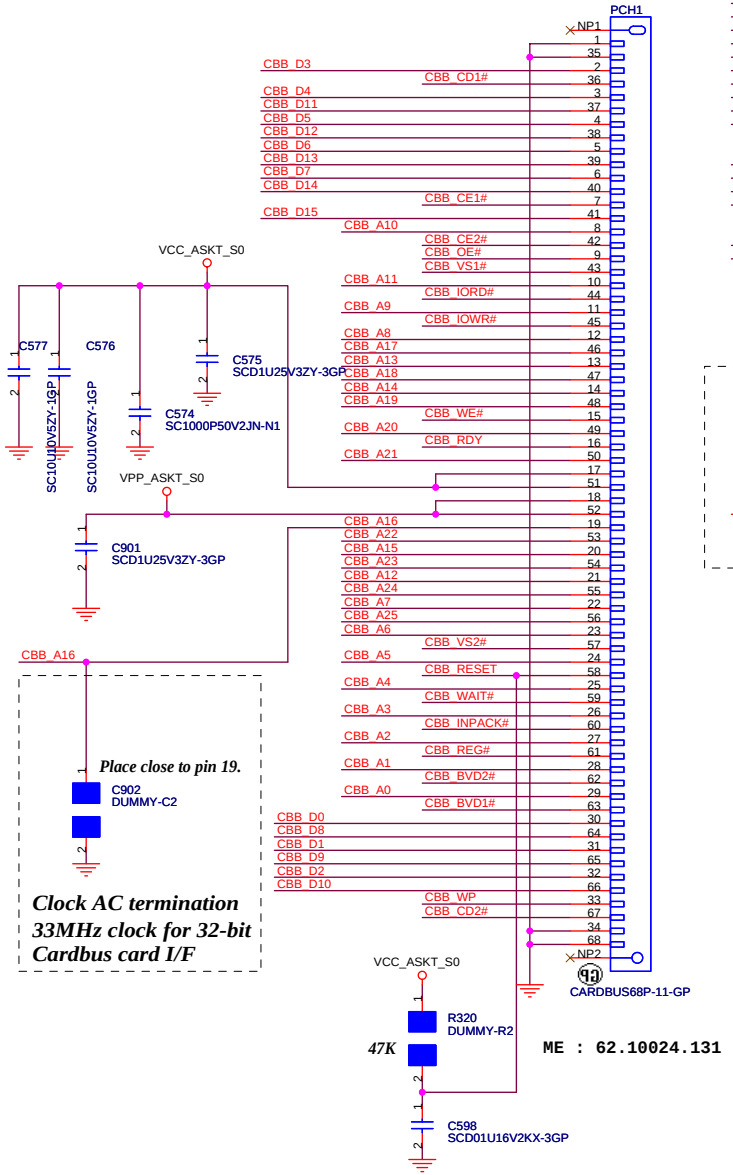
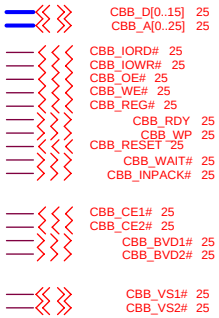
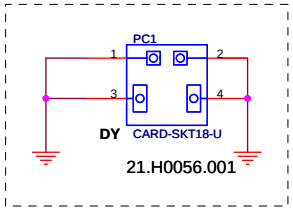
PCMCIA Socket



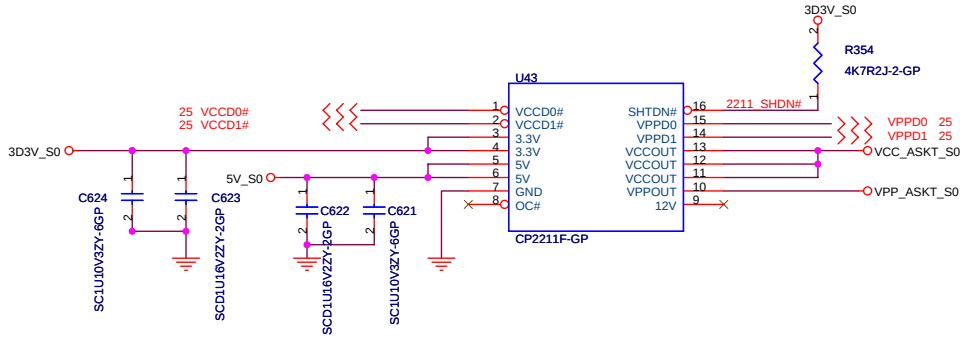
Cardbus I/F

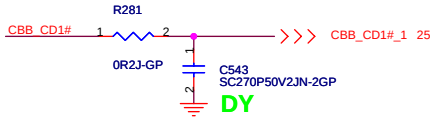


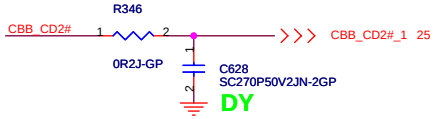


ME : 21.H0056.001

Power switch







<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCMCA / 1394 / CARD READER	
Size A3	Document Number Bolsena-E	Rev SA
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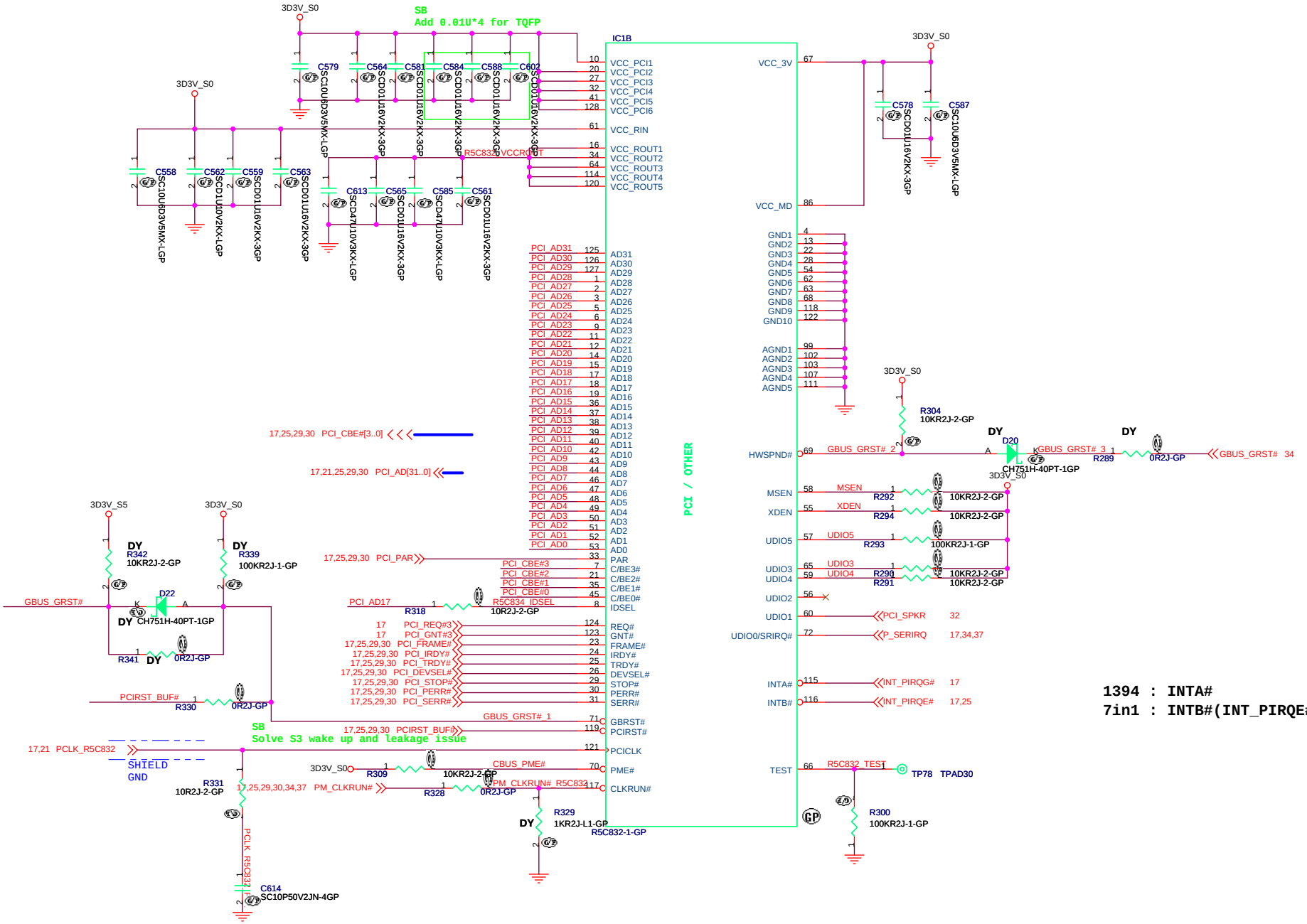
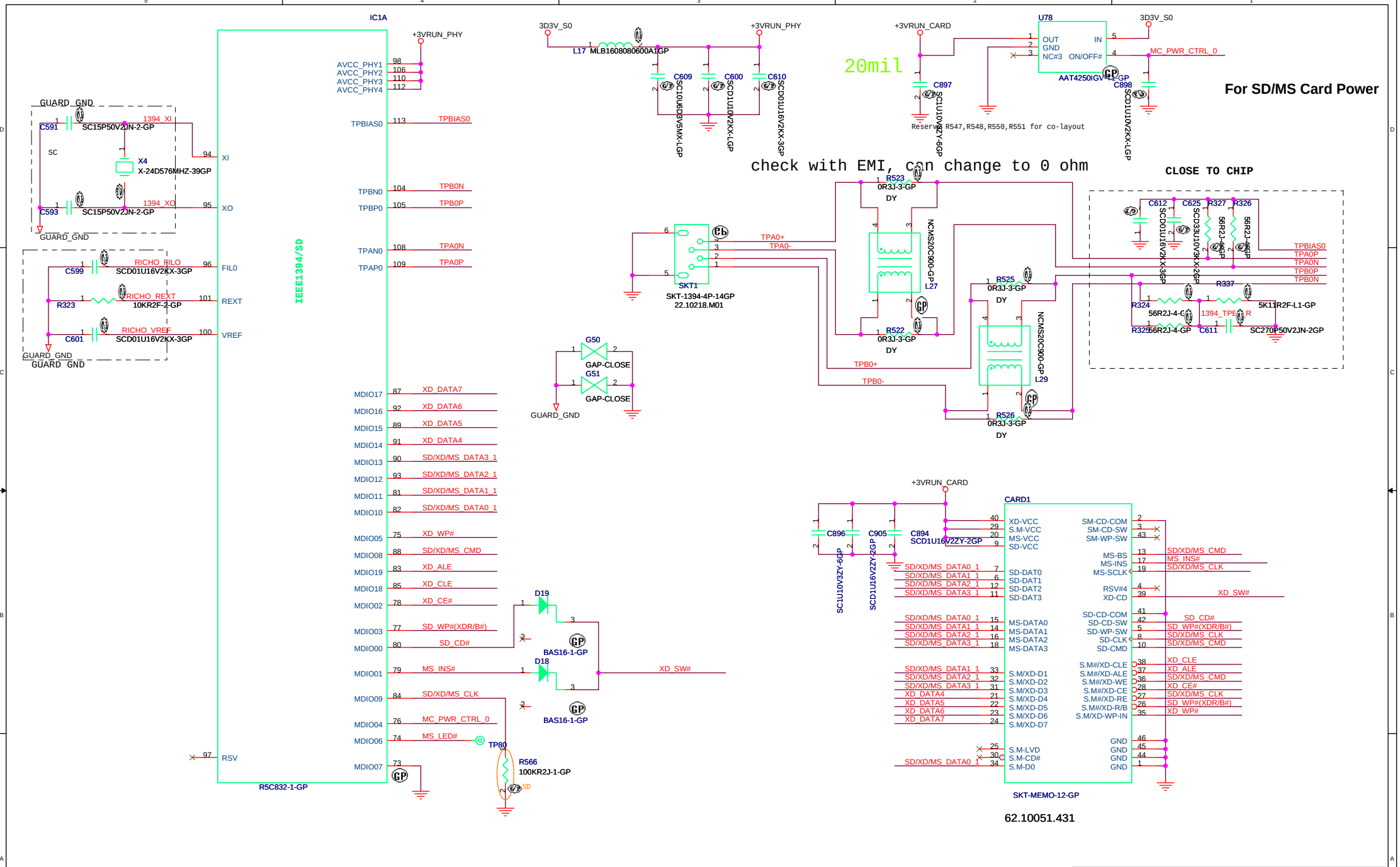


Solve S3 wake up and leakage issue

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***R5C832_1394_7IN1(2/2)***	
Size A3	Document Number **Bolsena-E**	Rev **SA**
Date: Thursday, October 13, 2005	Sheet 27 of 58	



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***R5C832_1394_7IN1(2/2)***	
Size A3	Document Number **Bolsena-E**	Rev **SA**
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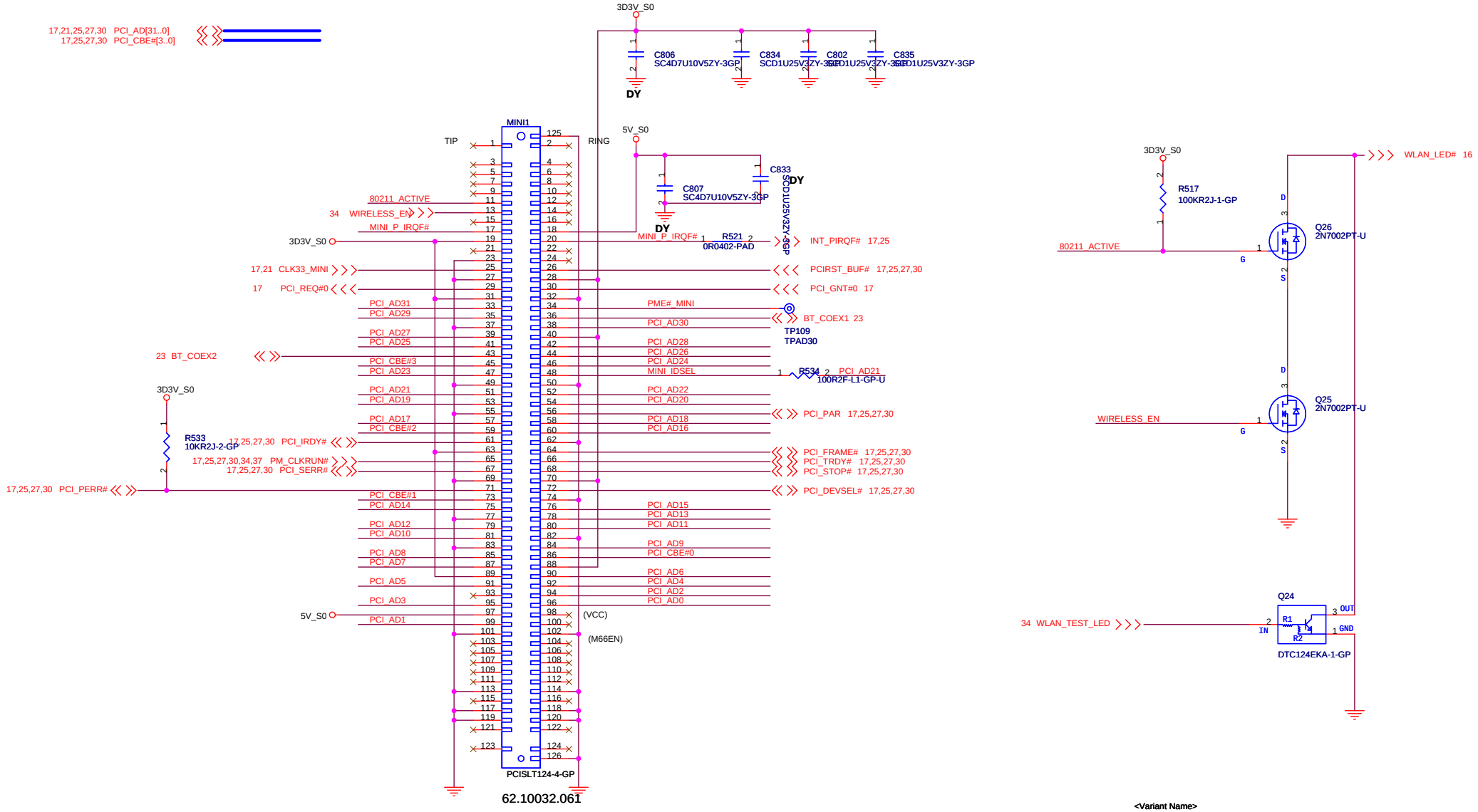
MINI-PCI



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**MINI-PCI**
Size A3	Document Number **Bolsena-E** Rev SA
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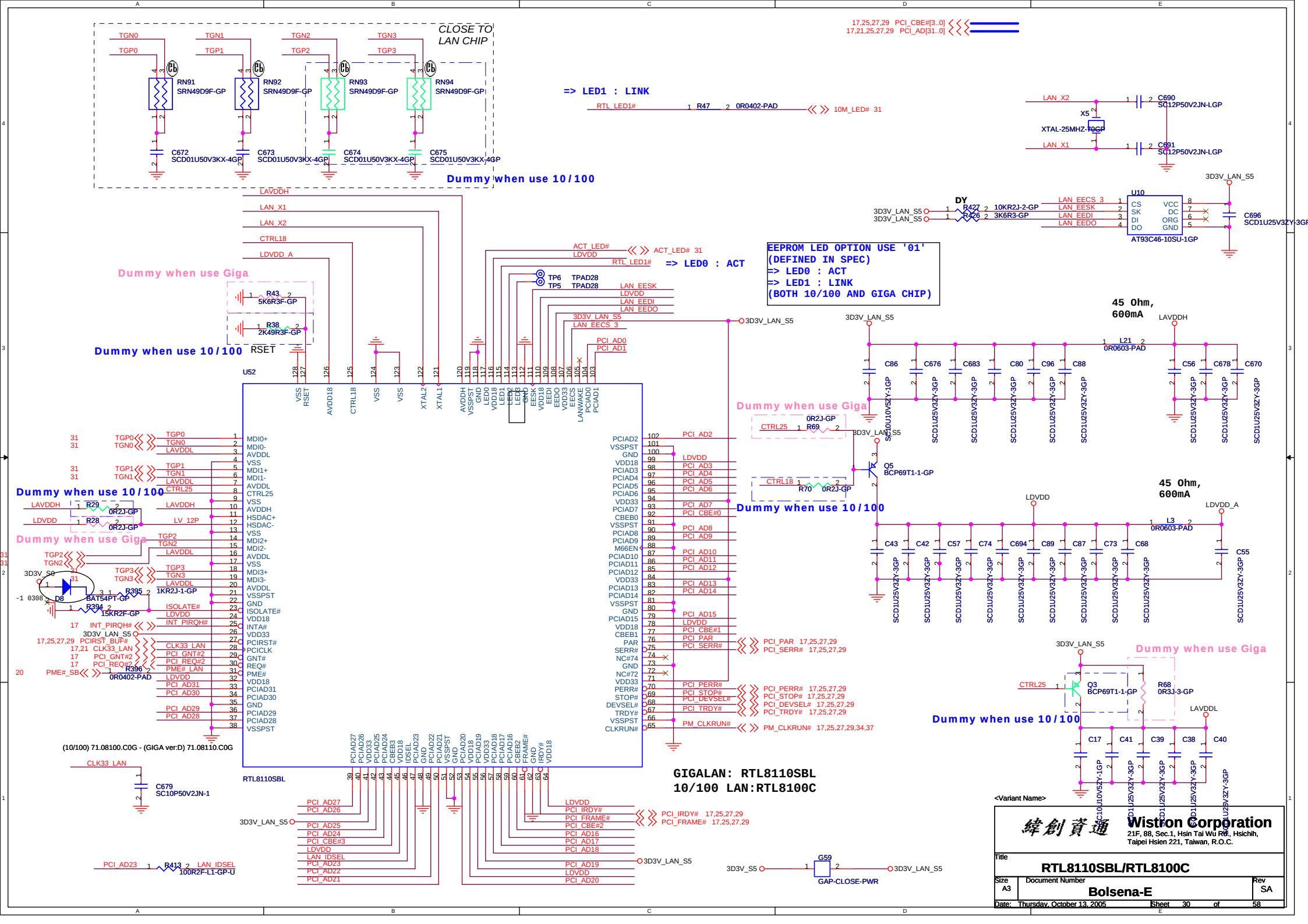
CLOSE TO LAN CHIP
TGN0
TGP0
TGN1
TGP1
TGN2
TGP2
TGN3
TGP3
RN91 SRN49D9F-GP
RN92 SRN49D9F-GP
RN93 SRN49D9F-GP
RN94 SRN49D9F-GP
C672 SCD01U50V3KX-4GP
C673 SCD01U50V3KX-4GP
C674 SCD01U50V3KX-4GP
C675 SCD01U50V3KX-4GP
Dummy when use 10/100
=> LED1 : LINK
RTL_LED1#
R47 0R0402-PAD
10M_LED# 31
17,25,27,29 PCI_CBE#[3..0]
17,21,25,27,29 PCI_AD[31..0]
LAN_X2
X5
XTAL-25MHZ-70GP
LAN_X1
C690 SC12P50V2JN-LGP
C691 SC12P50V2JN-LGP
3D3V_LAN_S5
DY
R427 10KR2J-2-GP
R426 3K6R3-GP
LAN_EECS_3
LAN_EESK
LAN_EEDI
LAN_EEDO
U10
CS
SK
DI
DO
VCC
DC
ORG
GND
AT93C46-10SU-1GP
C696 SCD1U25V3ZY-3GP
LAVDDH
LAN_X1
LAN_X2
CTRL18
LDVDD_A
Dummy when use Giga
R43 5K6R3F-GP
R38 2K49R3F-GP
Dummy when use 10/100
RSET
ACT_LED#
LDVDD
RTL_LED1#
ACT_LED# 31
=> LED0 : ACT
TP6 TPAD28
TP5 TPAD28
LAN_EESK
LDVDD
LAN_EEDI
LAN_EEDO
3D3V_LAN_S5
LAN_EECS_3
PCI_AD0
PCI_AD1
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
45 Ohm, 600mA
L21 0R0603-PAD
C86 C676 C683 C80 C96 C88
C56 C678 C670
SCD1U10V5ZY-1GP
SCD1U25V3ZY-3GP
U52
VSS RSET AVDDD18 CTRL18 VSS VSS XTAL2 XTAL1 AVDDH VSSPST GND LED0 VDD18 LED1 LED2 LED3 GND EESK VDD18 EEDI EEDO VDD33 EECS LANWAKE PCIAD0 PCIAD1
MDI0+ MDI0- AVDDL VSS MDI1+ MDI1- AVDDL CTRL25 VSS AVDDH HSDAC+ HSDAC- VSS MDI2+ MDI2- AVDDL VSS MDI3+ MDI3- AVDDL VSSPST GND ISOLATE# VDD18 INTA# VDD33 PCIRST# PCICLK GNT# REQ# PME# VDD18 PCIAD31 PCIAD30 GND PCIAD29 PCIAD28 VSSPST
PCIAD2 VSSPST GND VDD18 PCIAD3 PCIAD4 PCIAD5 PCIAD6 VDD33 PCIAD7 CBEB0 VSSPST PCIAD8 PCIAD9 M66EN PCIAD10 PCIAD11 PCIAD12 VDD33 PCIAD13 PCIAD14 VSSPST GND PCIAD15 VDD18 CBEB1 PAR SERR# NC#74 GND NC#72 VDD33 PERR# STOP# DEVSEL# TRDY# VSSPST CLKRUN#
PCIAD27 PCIAD26 VDD33 PCIAD25 PCIAD24 CBEB3 VDD18 IDSEL PCIAD23 GND PCIAD22 PCIAD21 VSSPST GND PCIAD20 VDD18 PCIAD19 VDD33 PCIAD18 PCIAD17 PCIAD16 CBEB2 FRAME# GND IRDY# VDD18
RTL8110SBL
TGP0 TGN0 LAVDDL
TGP1 TGN1 LAVDDL
LAVDDH R29 0R2J-GP
LDVDD R28 0R2J-GP
LV_12P
TGP2 TGN2 LAVDDL
TGP3 TGN3 LAVDDL
3D3V_S0
D8 BAT54PT-GP
R395 1KR2J-1-GP
R394 15KR2F-GP
ISOLATE# LDVDD INT_PIRQH#
INT_PIRQH#
3D3V_LAN_S5
PCIRST_BUF#
CLK33_LAN
PCI_GNT#2
PCI_REQ#2
PME#_LAN
R396 0R0402-PAD
PME#_SB
LDVDD
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD2
LDVDD
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_CBE#0
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
LDVDD
PCI_CBE#1
PCI_PAR
PCI_SERR#
PCI_PAR 17,25,27,29
PCI_SERR# 17,25,27,29
PCI_PERR#
PCI_STOP#
PCI_DEVSEL#
PCI_TRDY#
PM_CLKRUN#
PCI_PERR# 17,25,27,29
PCI_STOP# 17,25,27,29
PCI_DEVSEL# 17,25,27,29
PCI_TRDY# 17,25,27,29
PM_CLKRUN# 17,25,27,29,34,37
Dummy when use Giga
CTRL25 R69 0R2J-GP
CTRL18 R70 0R2J-GP
Q5 BCP69T1-1-GP
Dummy when use 10/100
45 Ohm, 600mA
LDVDD
LDVDD_A
L3 0R0603-PAD
C43 C42 C57 C74 C694 C89 C87 C73 C68
C55
SCD1U25V3ZY-3GP
Dummy when use Giga
CTRL25
Q3 BCP69T1-1-GP
R68 0R3J-3-GP
Dummy when use 10/100
LAVDDL
C17 C41 C39 C38 C40
(10/100) 71.08100.C0G - (GIGA ver:D) 71.08110.C0G
CLK33_LAN
C679 SC10P50V2JN-1
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_CBE#3
LDVDD
LAN_IDSEL
PCI_AD23
PCI_AD22
PCI_AD21
PCI_IRDY# 17,25,27,29
PCI_FRAME# 17,25,27,29
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD23
R413 100R2F-L1-GP-U
3D3V_S5
G59 GAP-CLOSE-PWR
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8110SBL/RTL8100C
Size A3
Document Number
Bolsena-E
Rev SA
Date: Thursday, October 13, 2005
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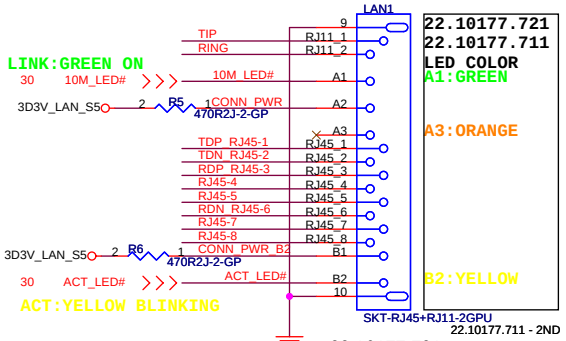
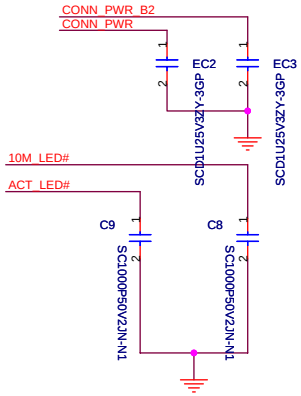
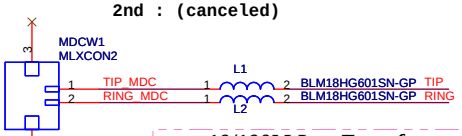
Link: Green - 10Mbps/802.11b Activity: Yellow
Orange - 100Mbps/802.11a
Yellow - 1Gbps



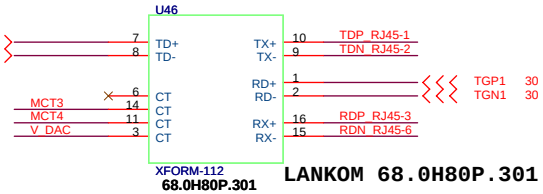
22.10177.721
ME : 22.10177.721
2nd : (canceled)



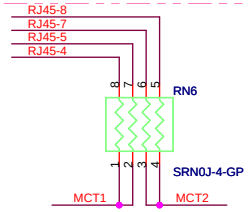


21.D0010.102
ME : 21.D0010.102

10/100M Lan Transformer



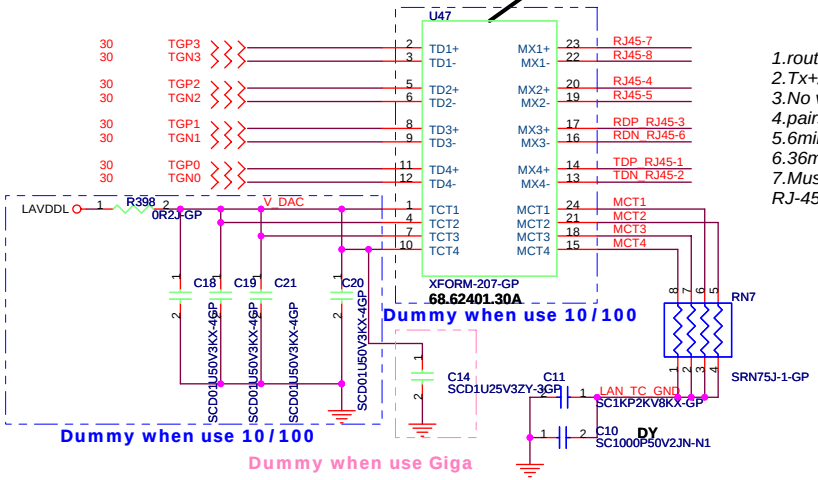
LANKOM 68.0H80P.301
Dummy when use Giga



GIGA Lan Transformer

LANKOM 68.02402.30A
netSWAP 68.62401.301 (GIGA ,Thick)

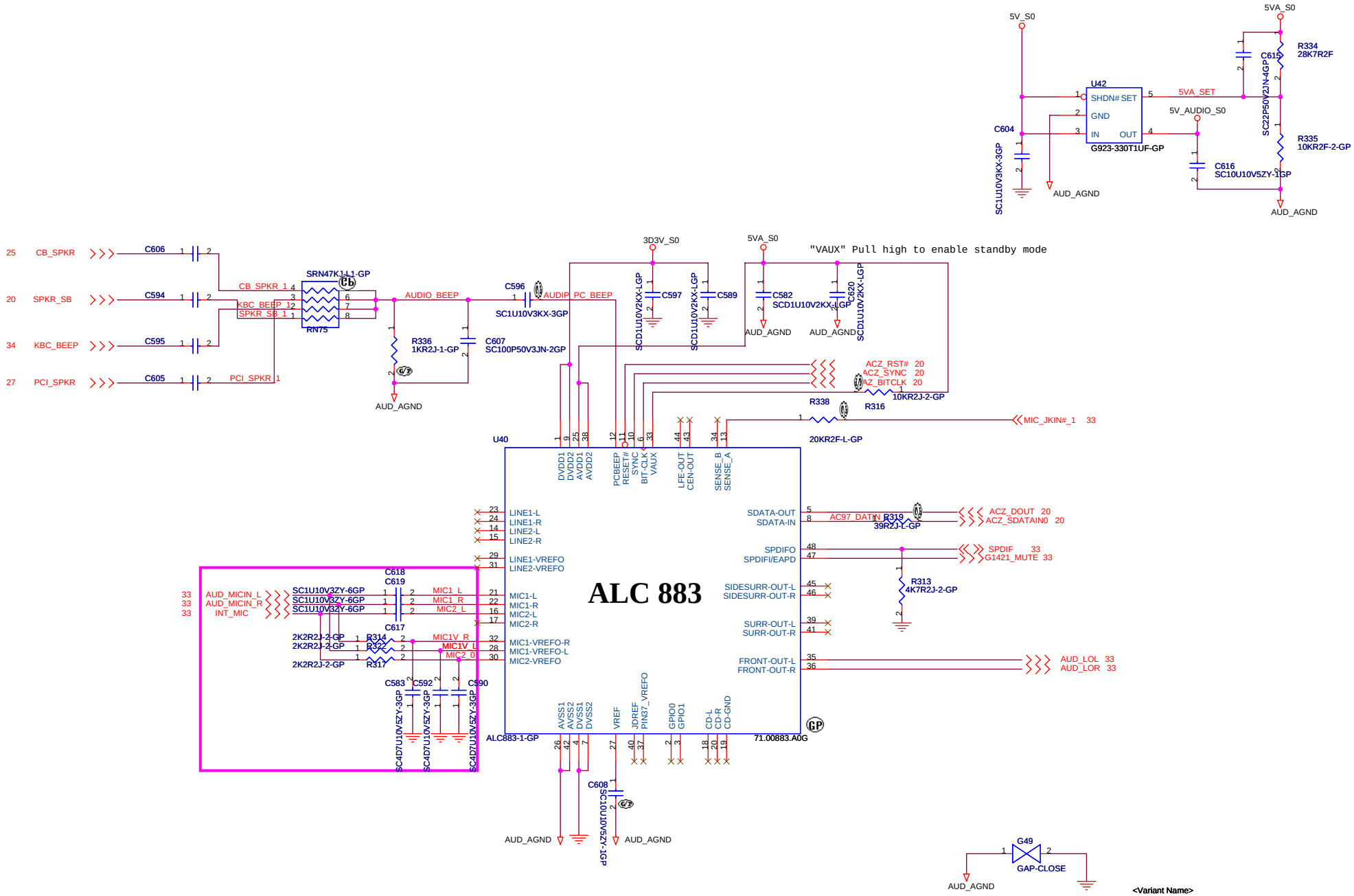
NETSWAP GIGA THICK PN IS 68.62401.301, DON'T USE NETSWAP THIN



Dummy when use 10/100
Dummy when use 10/100
Dummy when use Giga

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LAN CONN**	
Size A3	Document Number **Bolsena-E**	Rev SA
Date: Thursday, October 13, 2005	Sheet 31 of 58	



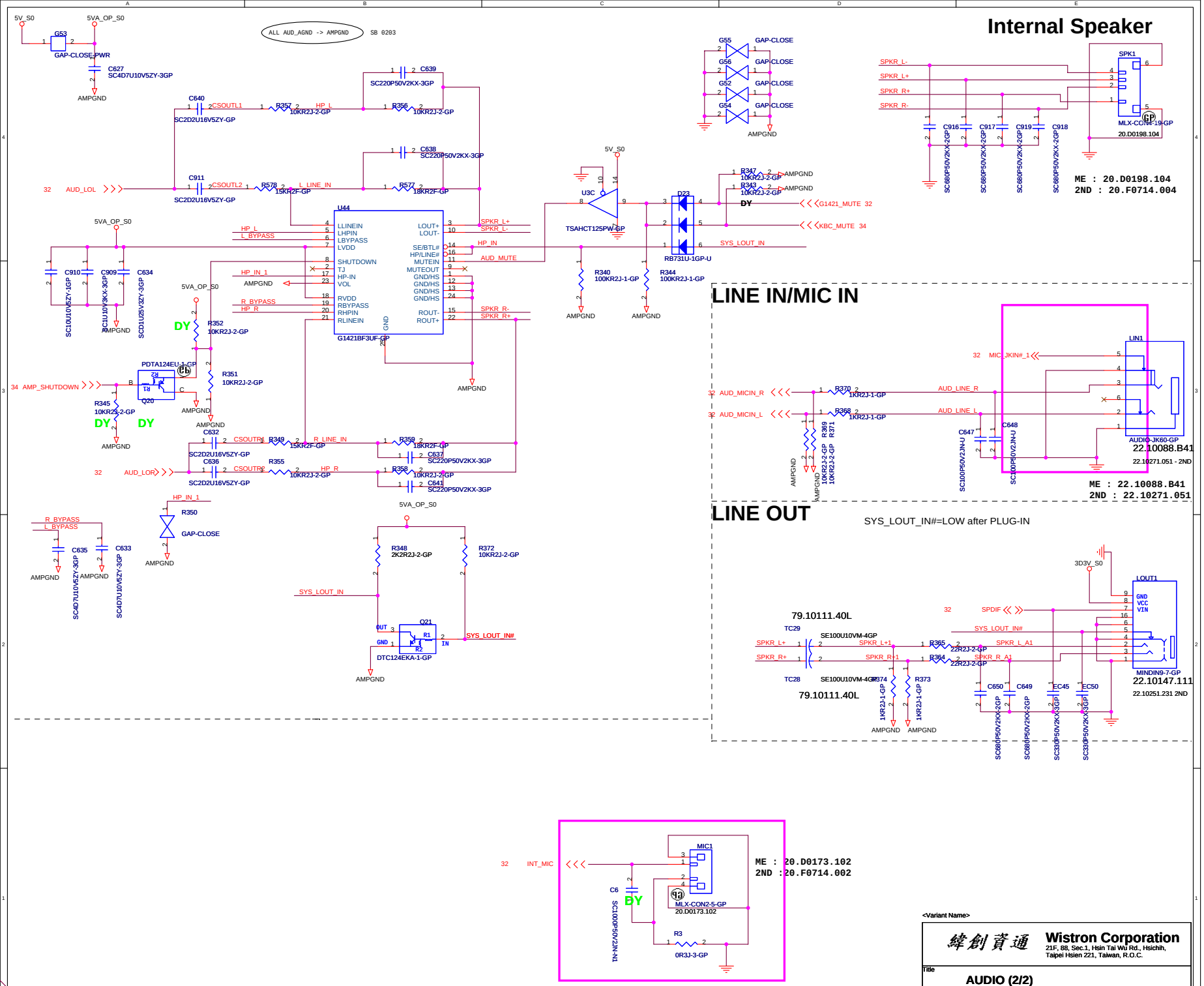
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO (1/2) -- CODEC ALC655**

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 32 of 58



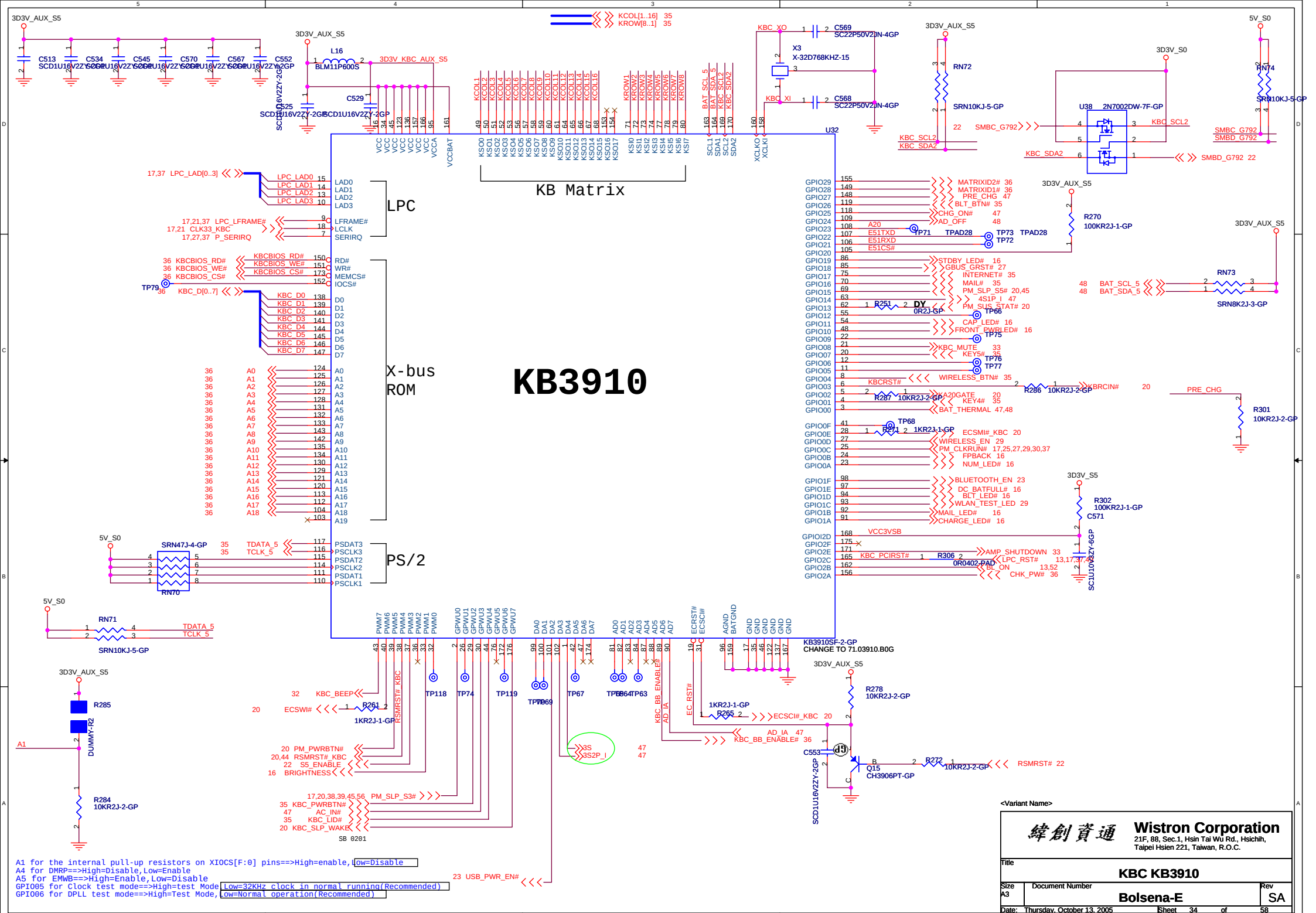
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: AUDIO (2/2)

Size: Custom | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 33 of 58


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
U32
KB3910SF-2-GP
CHANGE TO 71.03910.B0G
X3
X-32D768KHZ-15
U38 2N7002DW-7F-GP
Q15 CH3906PT-GP
RN72
SRN10KJ-5-GP
RN74
SRN10KJ-5-GP
RN73
SRN8K2J-3-GP
RN70
SRN47J-4-GP
RN71
SRN10KJ-5-GP
R285
DUMMY-R2
R284
10KR2J-2-GP
R270
100KR2J-1-GP
R301
10KR2J-2-GP
R302
100KR2J-1-GP
R278
10KR2J-2-GP
R272
10KR2J-2-GP
R286
10KR2J-2-GP
R287
10KR2J-2-GP
R291
1KR2J-1-GP
R261
1KR2J-1-GP
R265
1KR2J-1-GP
R306
0R0402-PAD
R251
0R2J-GP
DY
L16
BLM11P600S
3D3V_AUX_S5
3D3V_KBC_AUX_S5
3D3V_S0
5V_S0
KCOL[1..16] 35
KROW[8..1] 35
KBC_XO
KBC_XI
KBC_SCL2
KBC_SDA2
SMBC_G792
SMBD_G792
BAT_SCL_5
BAT_SDA_5
PRE_CHG
VCC3VSB
KBC_PCIRST#
KBCRST#
KBRCIN#
TDATA_5
TCLK_5
KBC_BEEP
ECSWI#
ECSCI#_KBC
KBC_BB_ENABLE#
AD_IA
EC_RST#
RSMRST#
PM_PWRBTN#
RSMRST#_KBC
S5_ENABLE
BRIGHTNESS
PM_SLP_S3#
KBC_PWRBTN#
AC_IN#
KBC_LID#
KBC_SLP_WAKE
USB_PWR_EN#
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
SB 0201
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC KB3910
Size A3
Document Number
Bolsena-E
Rev SA
Date: Thursday, October 13, 2005
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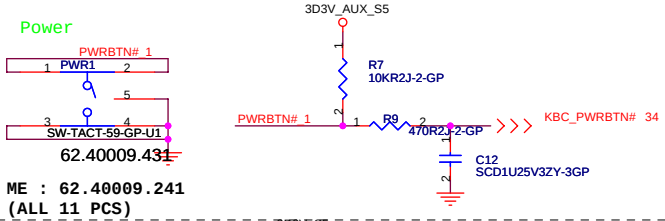
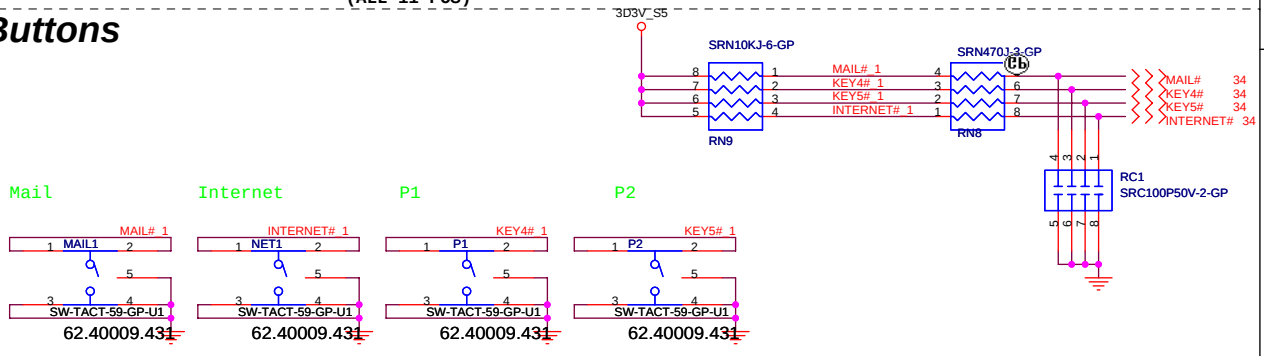
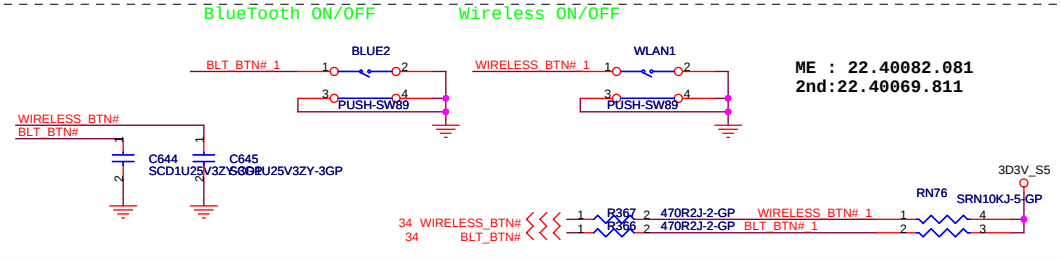
POWER BUTTON



ME : 62.40009.241
(ALL 11 PCS)

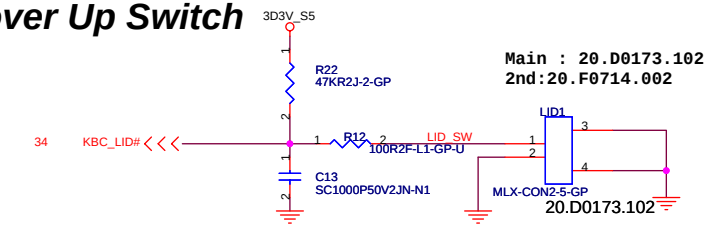
Buttons





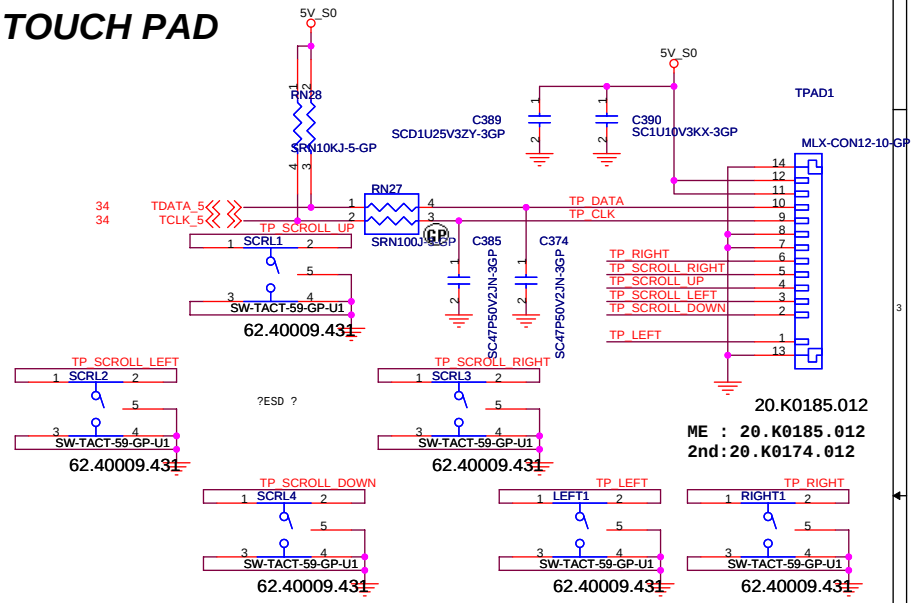
ME : 22.40082.081
2nd:22.40069.811

Cover Up Switch



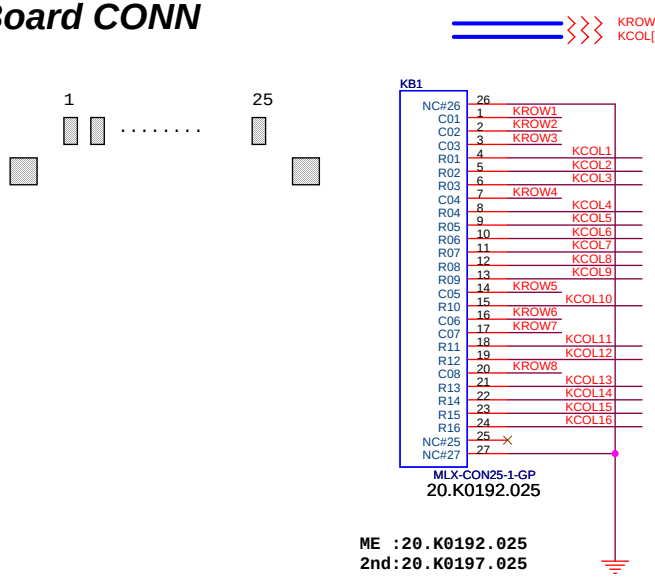
Main : 20.D0173.102
2nd:20.F0714.002

TOUCH PAD



20.K0185.012
ME : 20.K0185.012
2nd:20.K0174.012

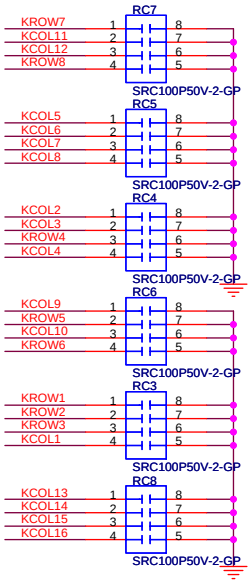
Internal KeyBoard CONN

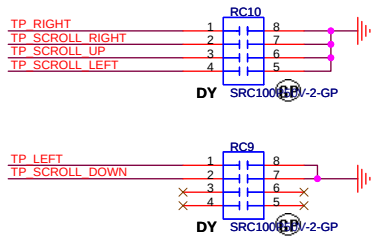


ME :20.K0192.025
2nd:20.K0197.025

Pin1 ==>*R01
Pin2 ==>*R02
Pin3 ==>*R03
Pin4 ==> C01
Pin5 ==> C02
Pin6 ==> C03
Pin7 ==>*R04
Pin8 ==> C04
Pin9 ==> C05
Pin10 ==> C06
Pin11 ==> C07
Pin12 ==> C08
Pin13 ==> C09
Pin14 ==>*R05
Pin15 ==> C10
Pin16 ==>*R06
Pin17 ==>*R07
Pin18 ==> C11
Pin19 ==> C12
Pin20 ==>*R08
Pin21 ==> C13
Pin22 ==> C14
Pin23 ==> C15
Pin24 ==> C16
Pin25 ==> NC

EMI Bypass cap.





<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BUTTONs / KB / TOUCHPAD	
Size A3	Document Number Bolsena-E	Rev SA
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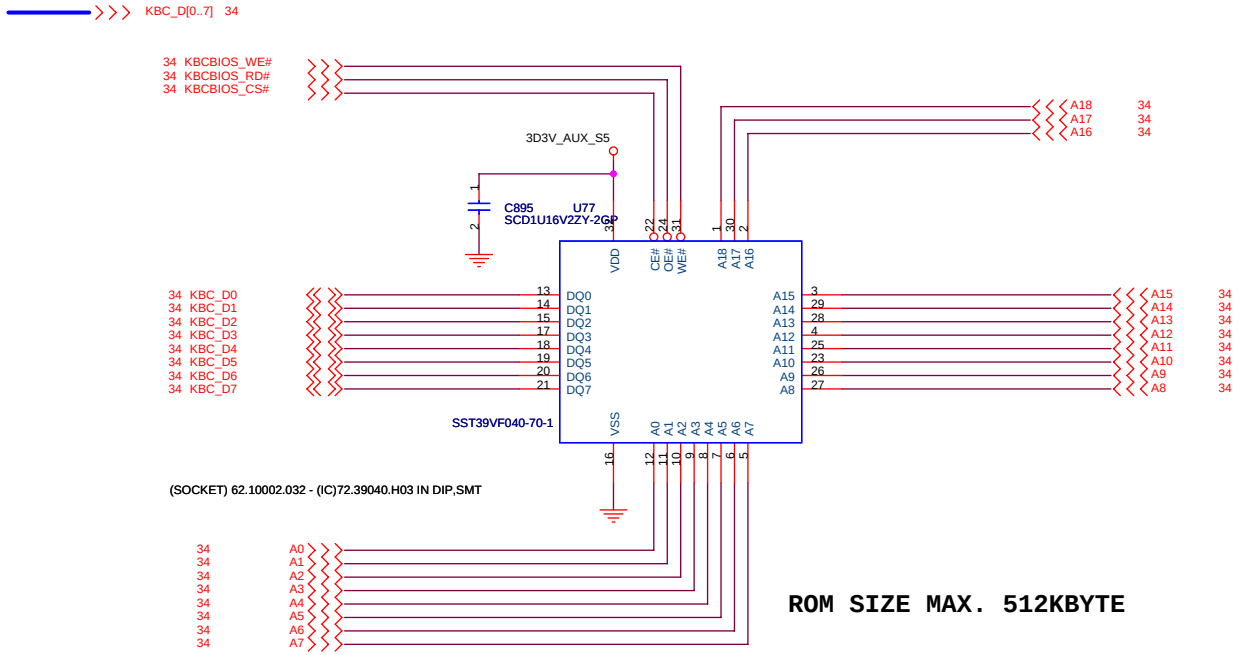
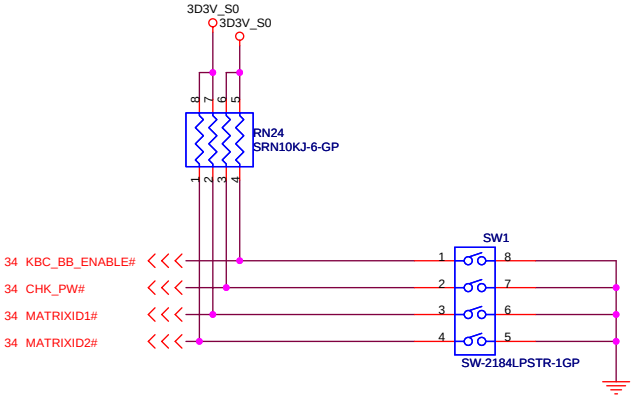


ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

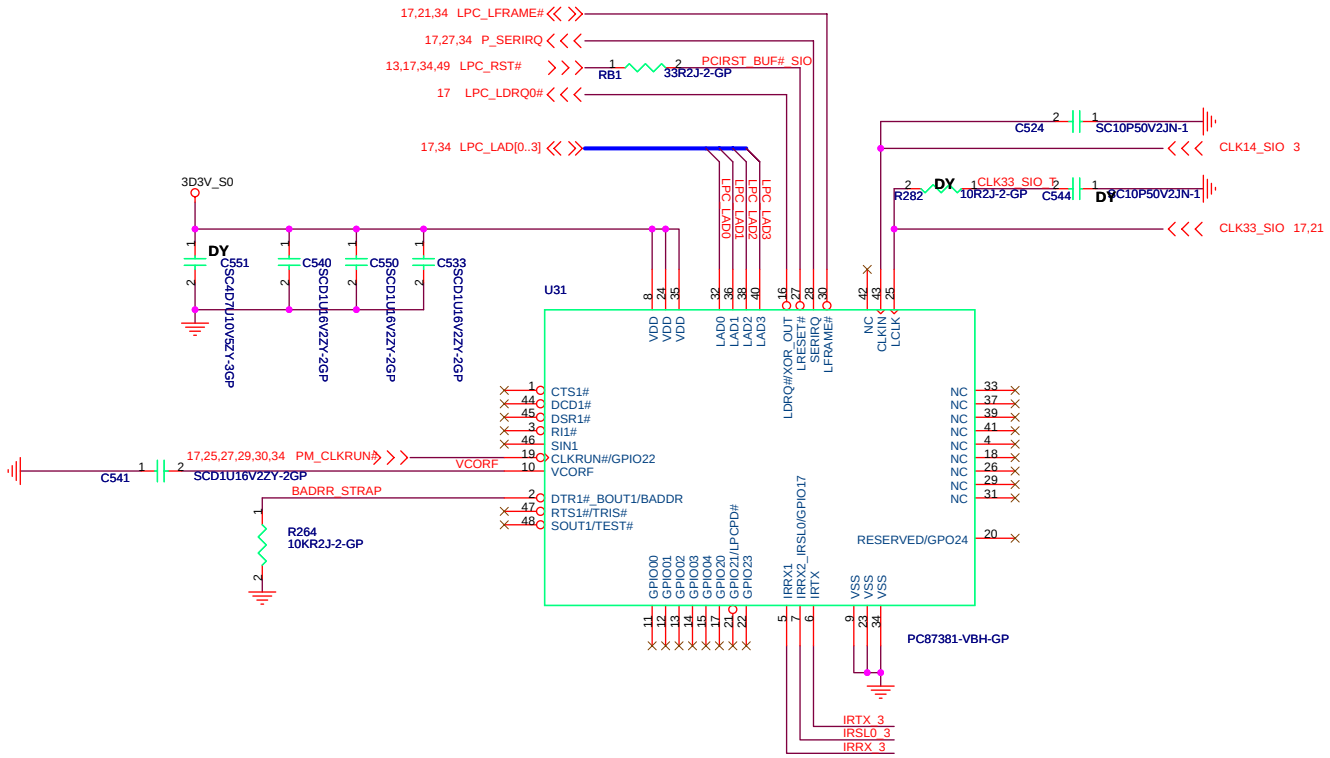
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

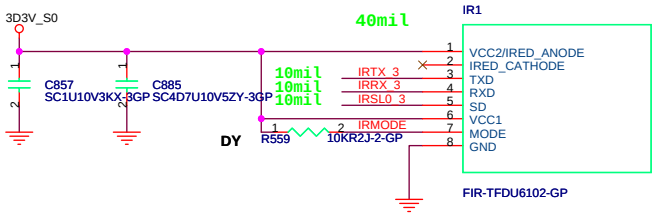
Title: **BIOS ROM**

Size: A3 | Document Number: **Bolsena-E** | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 36 of 58



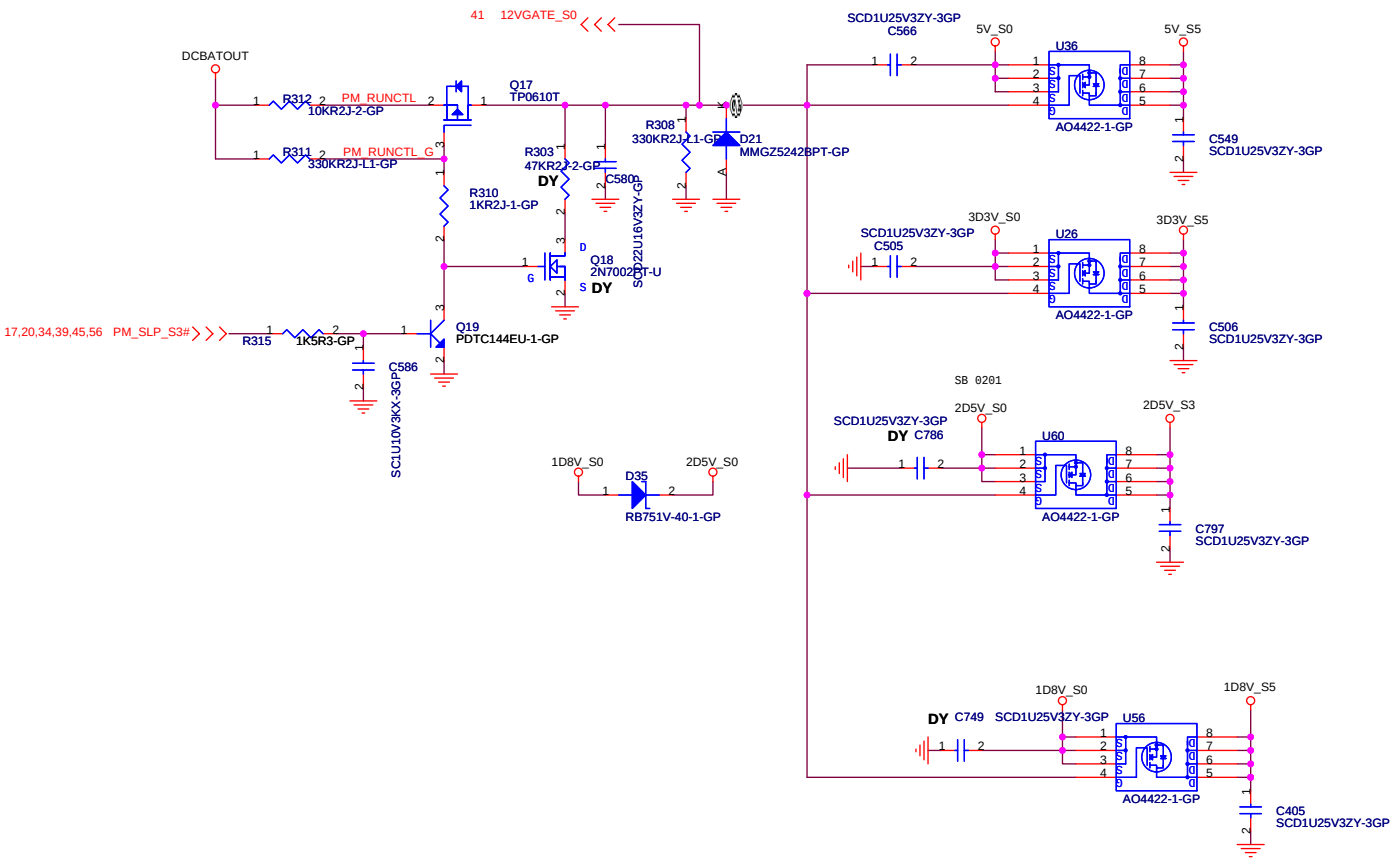
Infineon FIR Module



56.15001.051

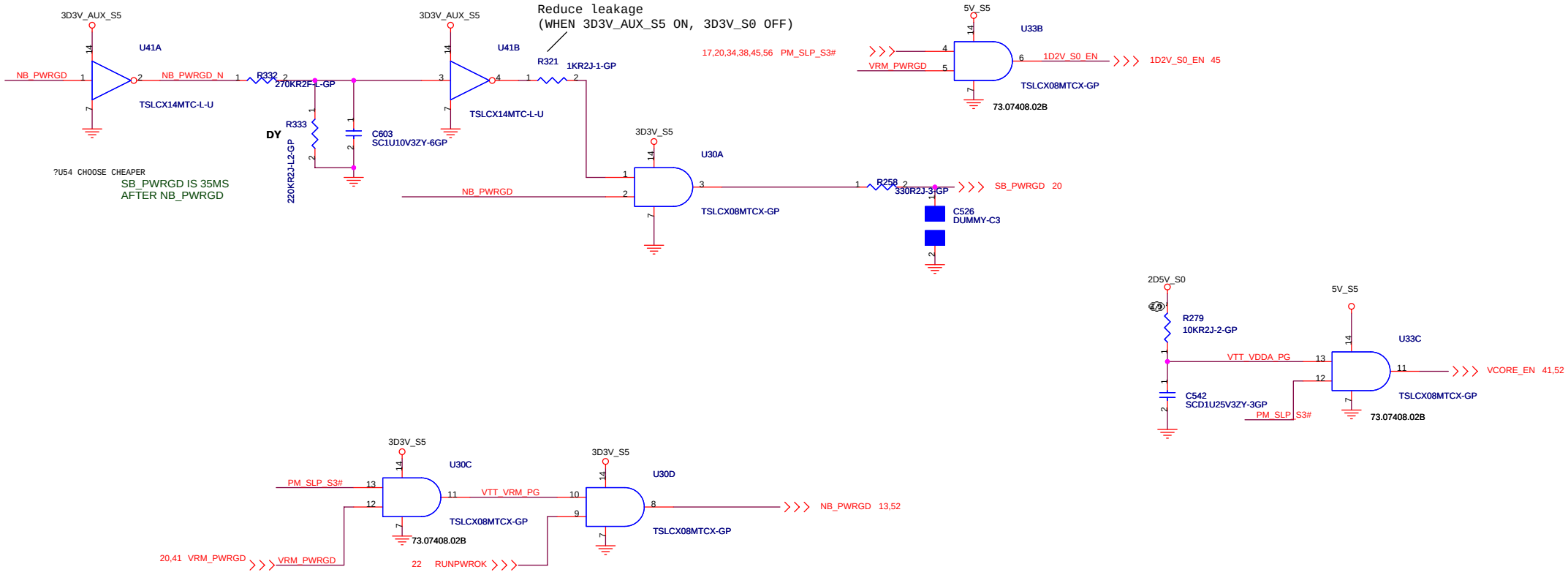
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**SUPER IO NC87381**	
Size A3	Document Number **SNIPE**	Rev -2
Date: Thursday, October 13, 2005	Sheet 37 of 58	

Run Power



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**PWR CTL LOGIC / PWR PLANE**	
Size A3	Document Number **Bolsena-E**	Rev SA
Date: Thursday, October 13, 2005	Sheet 38 of 58	



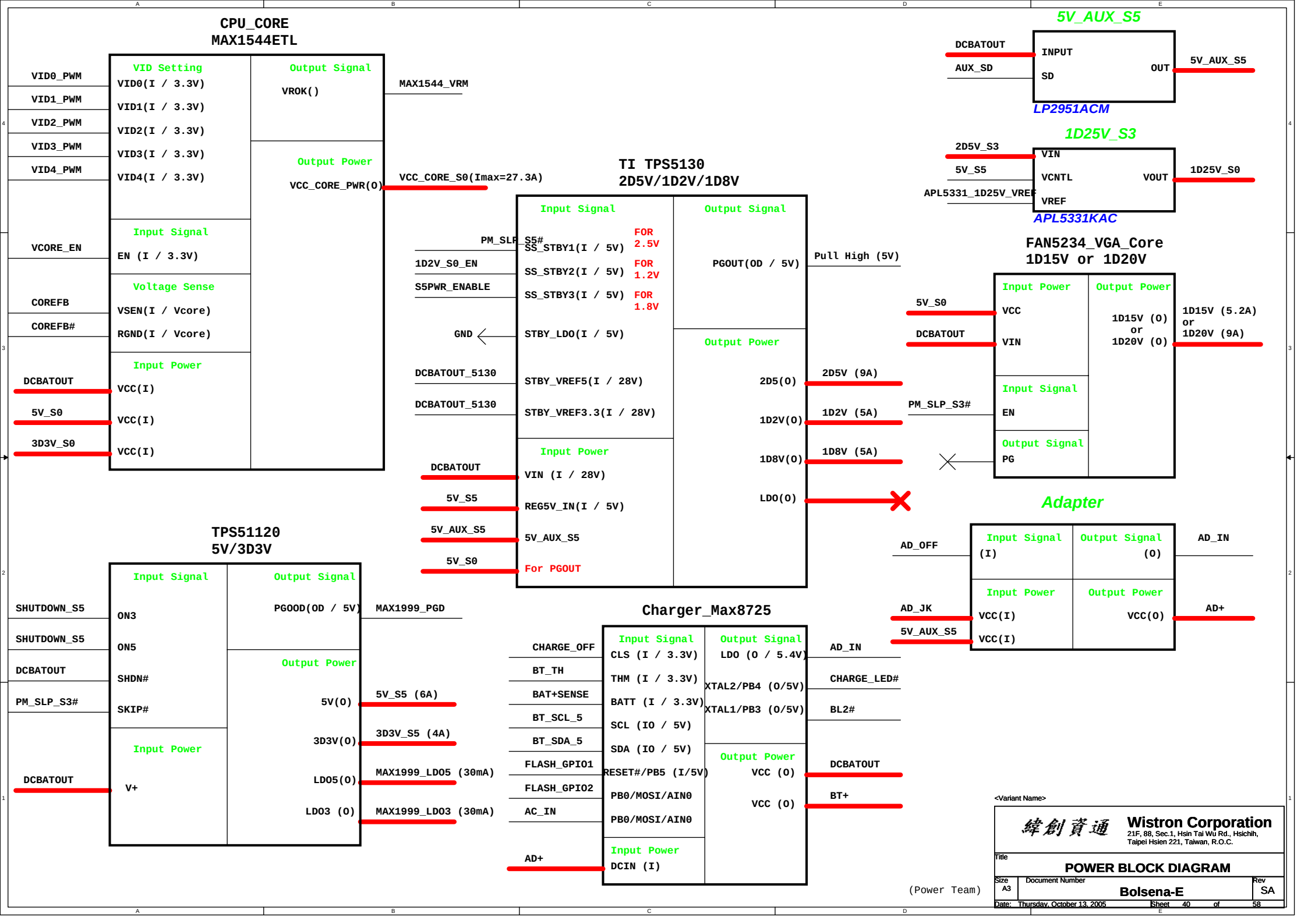
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWERGOOD&ENABLES**

Size	Document Number	Rev
Custom	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 39 of 58


CPU_CORE
MAX1544ETL
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Output Signal
VROK()
Output Power
VCC_CORE_PWR(O)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
VID0_PWM
VID1_PWM
VID2_PWM
VID3_PWM
VID4_PWM
VCORE_EN
COREFB
COREFB#
DCBATOUT
5V_S0
3D3V_S0
MAX1544_VRM
VCC_CORE_S0(Imax=27.3A)
TI TPS5130
2D5V/1D2V/1D8V
Input Signal
SS_STBY1(I / 5V)
SS_STBY2(I / 5V)
SS_STBY3(I / 5V)
STBY_LDO(I / 5V)
STBY_VREF5(I / 28V)
STBY_VREF3.3(I / 28V)
Input Power
VIN (I / 28V)
REG5V_IN(I / 5V)
5V_AUX_S5
For PGOUT
Output Signal
PGOUT(OD / 5V)
Output Power
2D5(O)
1D2V(O)
1D8V(O)
LDO(O)
FOR 2.5V
FOR 1.2V
FOR 1.8V
PM_SLP_S5#
1D2V_S0_EN
S5PWR_ENABLE
GND
DCBATOUT_5130
DCBATOUT_5130
DCBATOUT
5V_S5
5V_AUX_S5
5V_S0
Pull High (5V)
2D5V (9A)
1D2V (5A)
1D8V (5A)
5V_AUX_S5
DCBATOUT
AUX_SD
INPUT
SD
OUT
LP2951ACM
1D25V_S3
2D5V_S3
5V_S5
APL5331_1D25V_VREF
VIN
VCNTL
VREF
VOUT
APL5331KAC
1D25V_S0
FAN5234_VGA_Core
1D15V or 1D20V
Input Power
VCC
VIN
Input Signal
EN
Output Signal
PG
Output Power
1D15V (O)
or
1D20V (O)
5V_S0
DCBATOUT
PM_SLP_S3#
1D15V (5.2A)
or
1D20V (9A)
Adapter
Input Signal
(I)
Output Signal
(O)
Input Power
VCC(I)
VCC(I)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN
AD+
TPS51120
5V/3D3V
Input Signal
ON3
ON5
SHDN#
SKIP#
Input Power
V+
Output Signal
PGOOD(OD / 5V)
Output Power
5V(O)
3D3V(O)
LDO5(O)
LDO3 (O)
SHUTDOWN_S5
SHUTDOWN_S5
DCBATOUT
PM_SLP_S3#
DCBATOUT
MAX1999_PGD
5V_S5 (6A)
3D3V_S5 (4A)
MAX1999_LDO5 (30mA)
MAX1999_LDO3 (30mA)
Charger_Max8725
Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0
Input Power
DCIN (I)
Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)
Output Power
VCC (O)
VCC (O)
CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN
AD+
AD_IN
CHARGE_LED#
BL2#
DCBATOUT
BT+
(Power Team)
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
POWER BLOCK DIAGRAM
Size
A3
Document Number
Bolsena-E
Rev
SA
Date: Thursday, October 13, 2005
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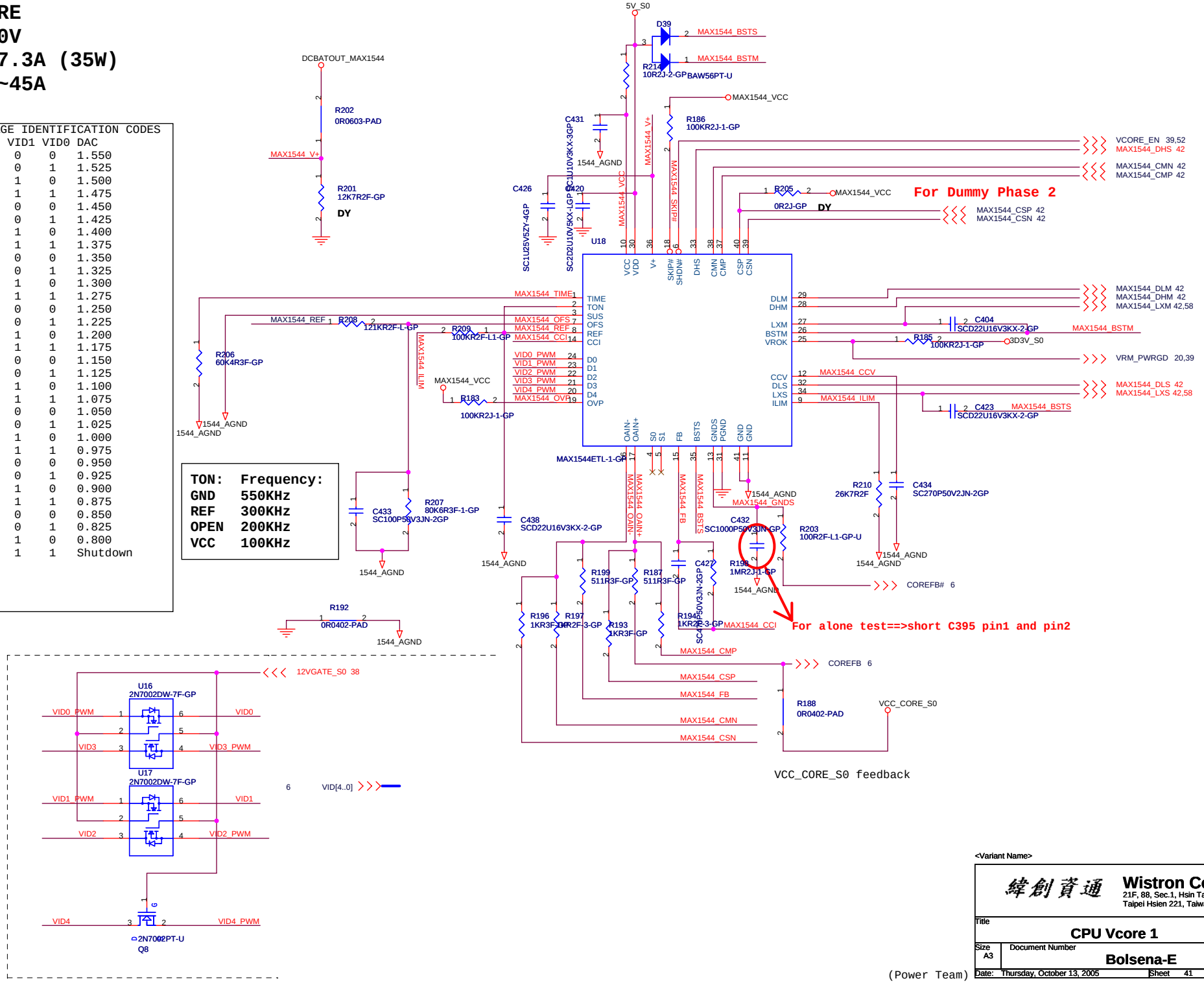
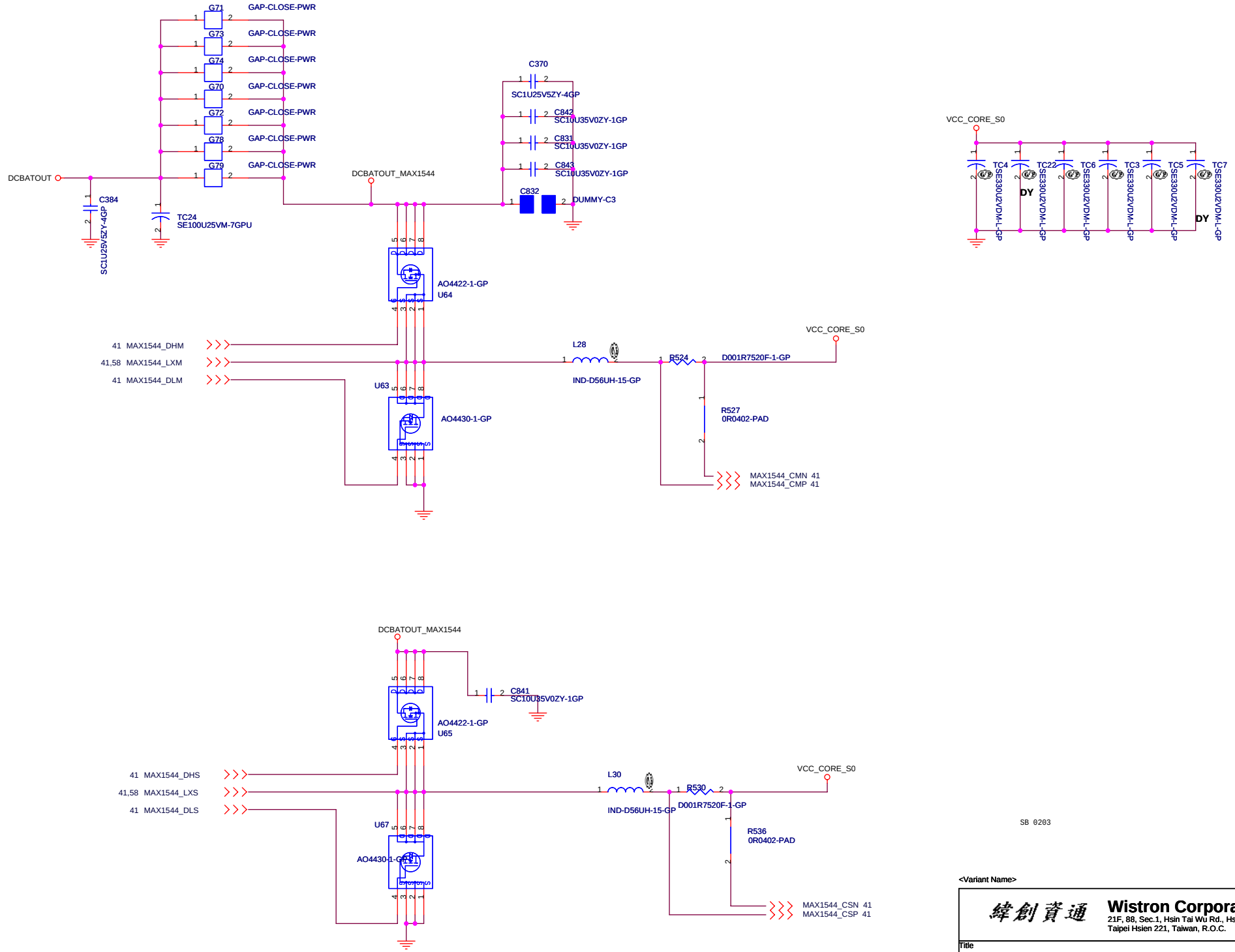
CPU_VCORE
VID=1.20V
Iomax=27.3A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

TON:	Frequency:
GND	550KHz
REF	300KHz
OPEN	200KHz
VCC	100KHz

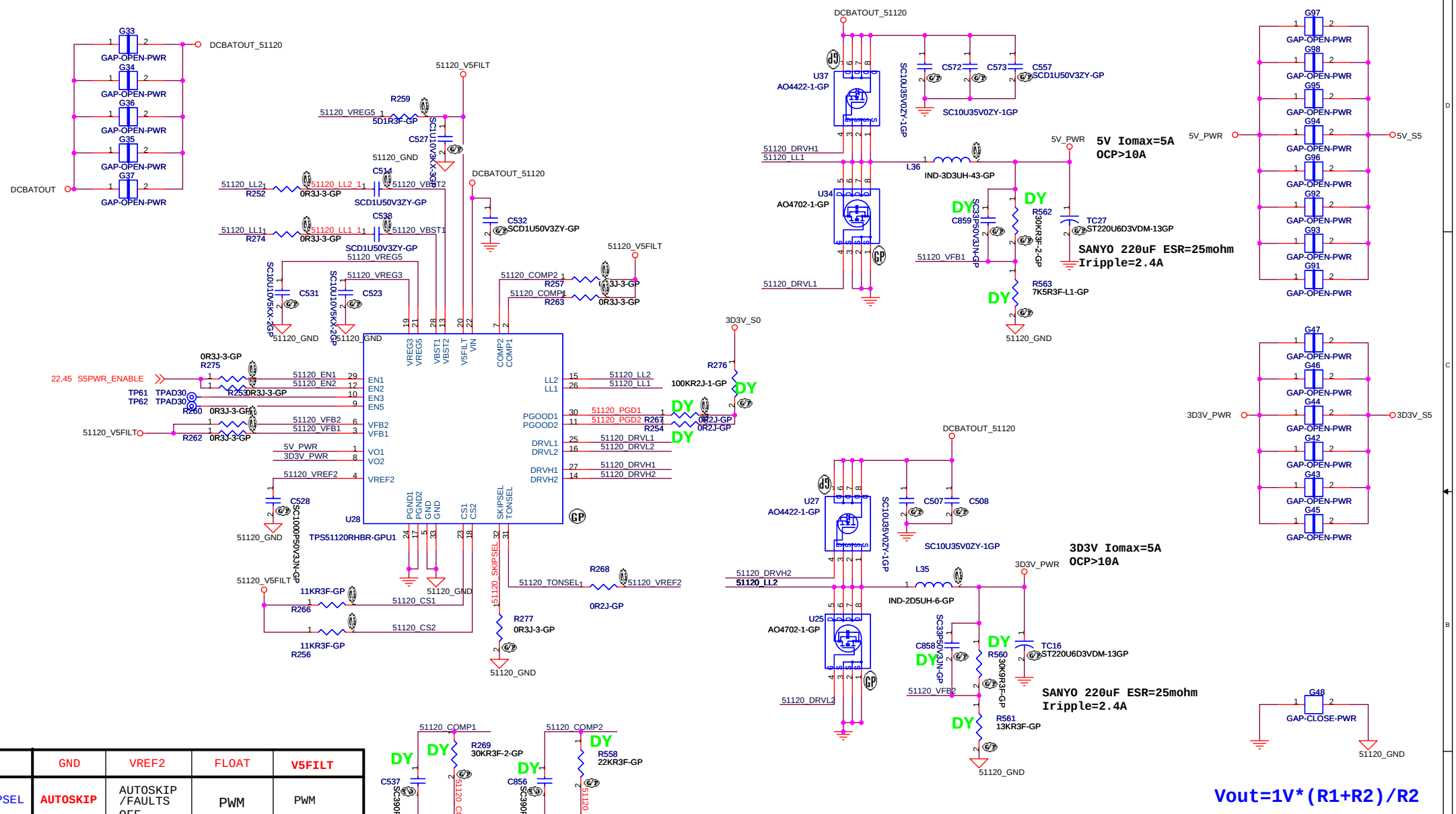




<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**CPU Vcore 2**	
Size A3	Document Number **Bolsena-E**	Rev SA
Date: Thursday, October 13, 2005	Sheet 42 of 58	



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

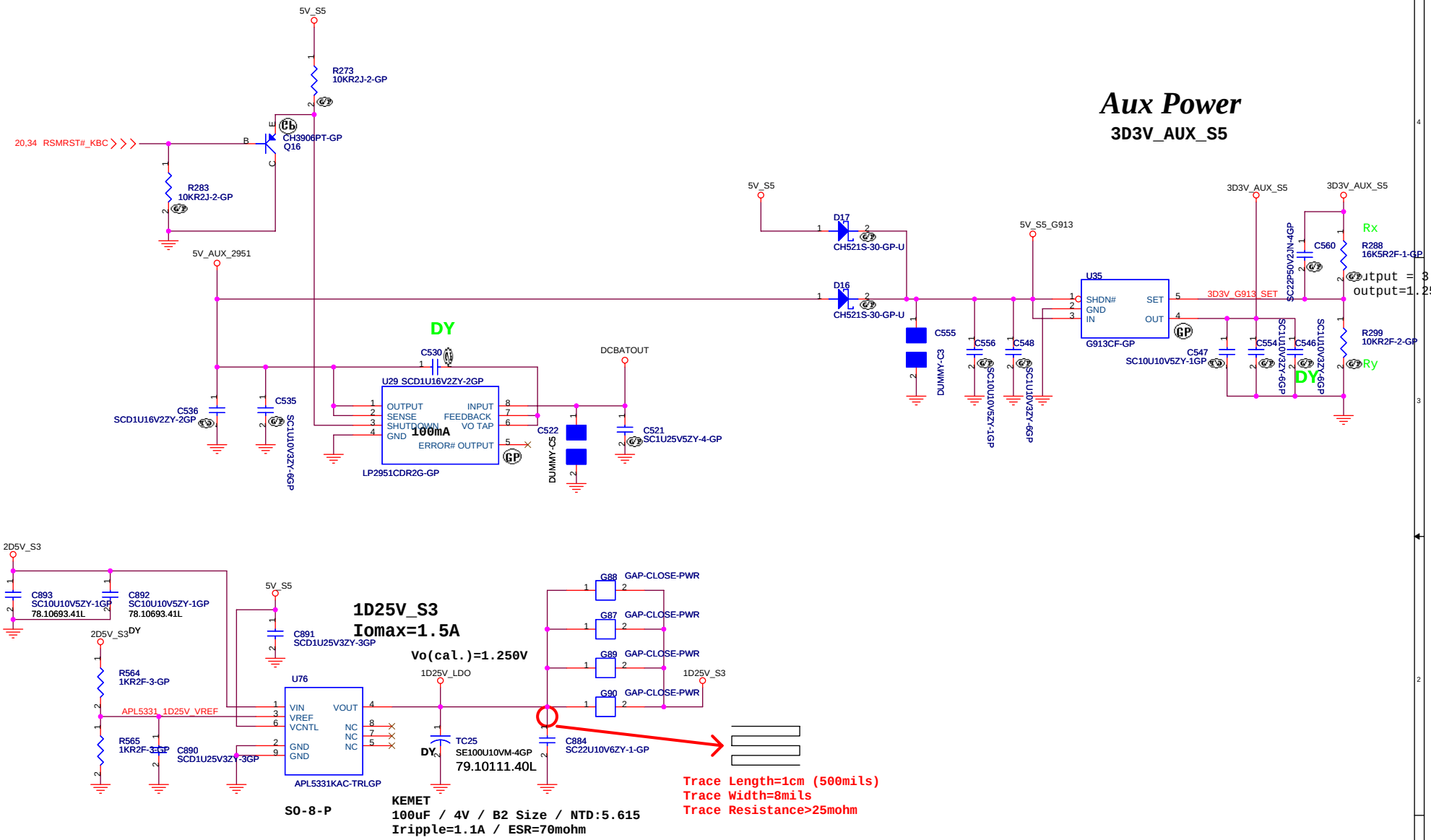
Title: TPS51120 / 3D3V / 5V

Size: A3 | Document Number: Bolsena-E | Rev: -1

Date: Thursday, October 13, 2005 | Sheet 43 of 58

Aux Power

3D3V_AUX_S5



SO-8-P

KEMET
100uF / 4V / B2 Size / NTD:5.615
Iripple=1.1A / ESR=70mohm

(Power Team)

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**1D2V_S3 / 3D3V_AUX**	
Size A3	Document Number **Bolsena-E**	Rev SA
Date: Thursday, October 13, 2005	Sheet 44 of 58	

TI TPS5130 for 2.5V, 1.2V, 1.8V

Vo=(R1*0.85)/R2+0.85

(1D2V=>CH1 , 1D8V=>CH2 , 2D5V =>CH3)

For 2.5V
SETTING=2.516V

For 1.8V
SETTING=1.8275V

For 1.2V
SETTING=1.2172V

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

T(soft)=1.736ms

1D2V_OCP
R180 11K3R2F-2-GP
C386 SCD1U25V3ZY-3GP
OCP
8.4A=>R226=13K
10A=>R226=22K

1D8V_OCP
R179 12K1R2F-L1-GP
C380 SCD1U25V3ZY-3GP
OCP
8.4A=>R229=12.65K
10A=>R229=22K

2D5V_OCP
R181 18KR2F-GP
C392 SCD1U25V3ZY-3GP
OCP
12A=>R225=18K
18A=>R225=28K

TPS5130

TPS5130PTRG4-GP-U

LDO SETTING

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS5130 1D2V/1D8V2D5V/ (1/2)

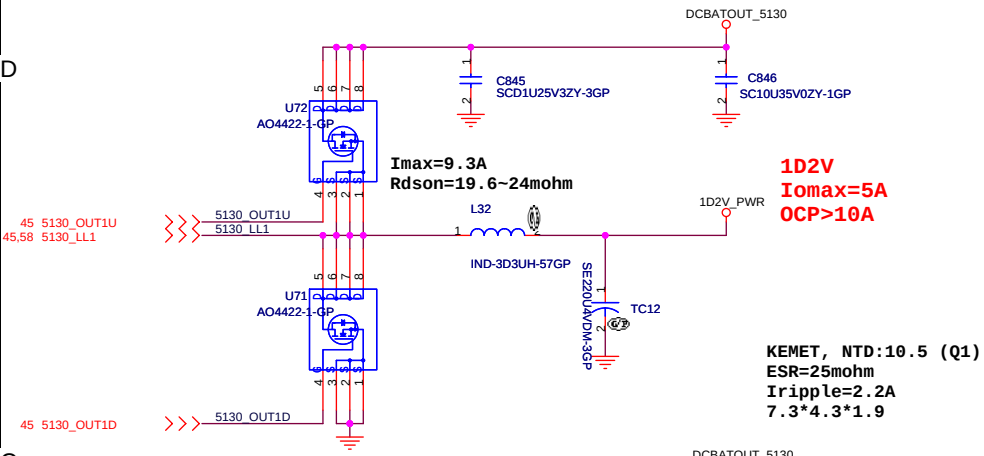
Size: A3 | Document Number: Bolsena-E | Rev: SA

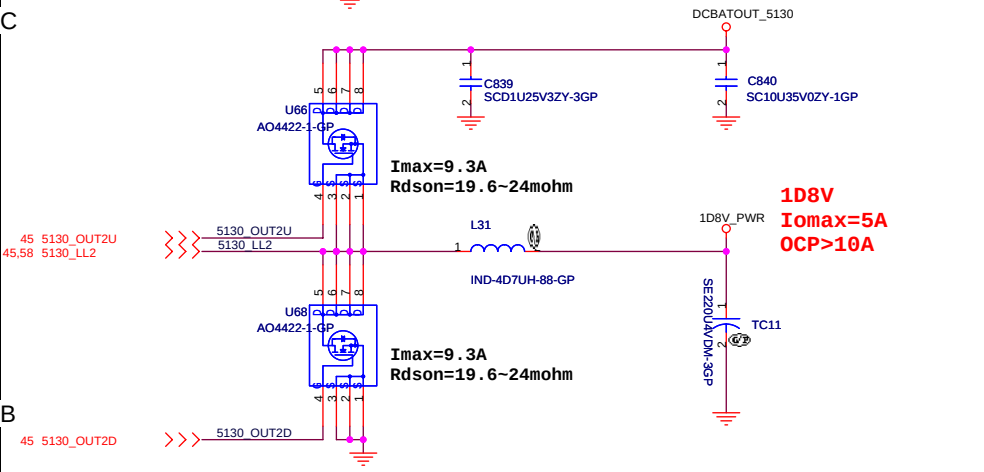
Date: Thursday, October 13, 2005 | Sheet 45 of 58

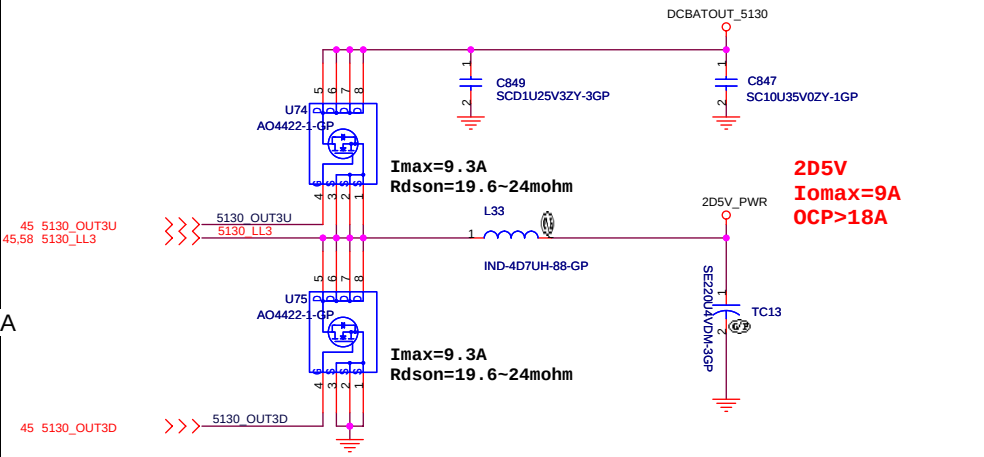
(Power Team)

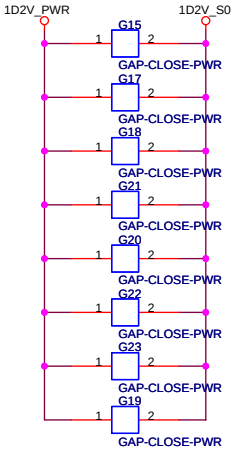
TI TPS5130 for 2D5V, 1D2V, 1D8V

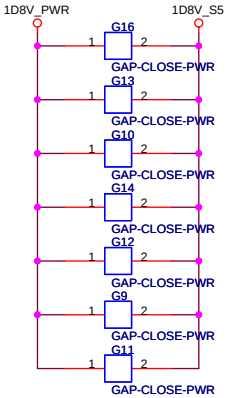
(1D2V=>CH1 , 1D8V=>CH2 , 2D5V =>CH3)

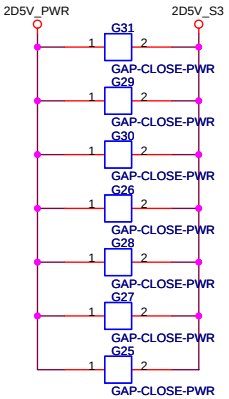












(Power Team)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
TPS5130 1D2V/1D8V2D5V/ (2/2)		
Size A3	Document Number Bolsena-E	Rev SA
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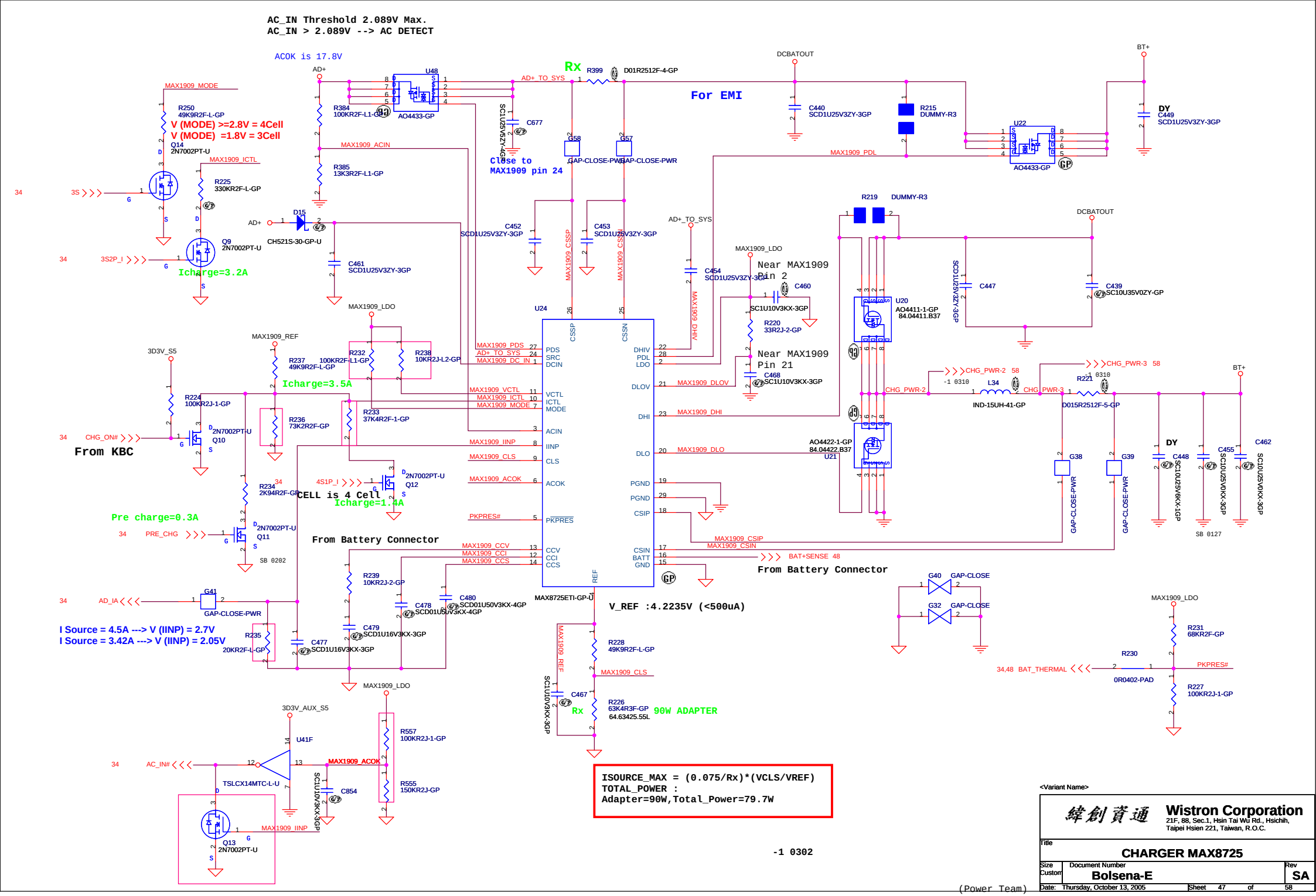
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
ACOK is 17.8V
V (MODE) >=2.8V = 4Cell
V (MODE) =1.8V = 3Cell
Icharge=3.2A
Icharge=3.5A
Icharge=1.4A
CELL is 4 Cell
Pre charge=0.3A
From KBC
From Battery Connector
I Source = 4.5A ---> V (IINP) = 2.7V
I Source = 3.42A ---> V (IINP) = 2.05V
Close to MAX1909 pin 24
Rx
For EMI
Near MAX1909 Pin 2
Near MAX1909 Pin 21
V_REF :4.2235V (<500uA)
90W ADAPTER
ISOURCE_MAX = (0.075/Rx)*(VCLS/VREF)
TOTAL_POWER :
Adapter=90W,Total_Power=79.7W
-1 0302
(Power Team)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8725
Bolsena-E
SA
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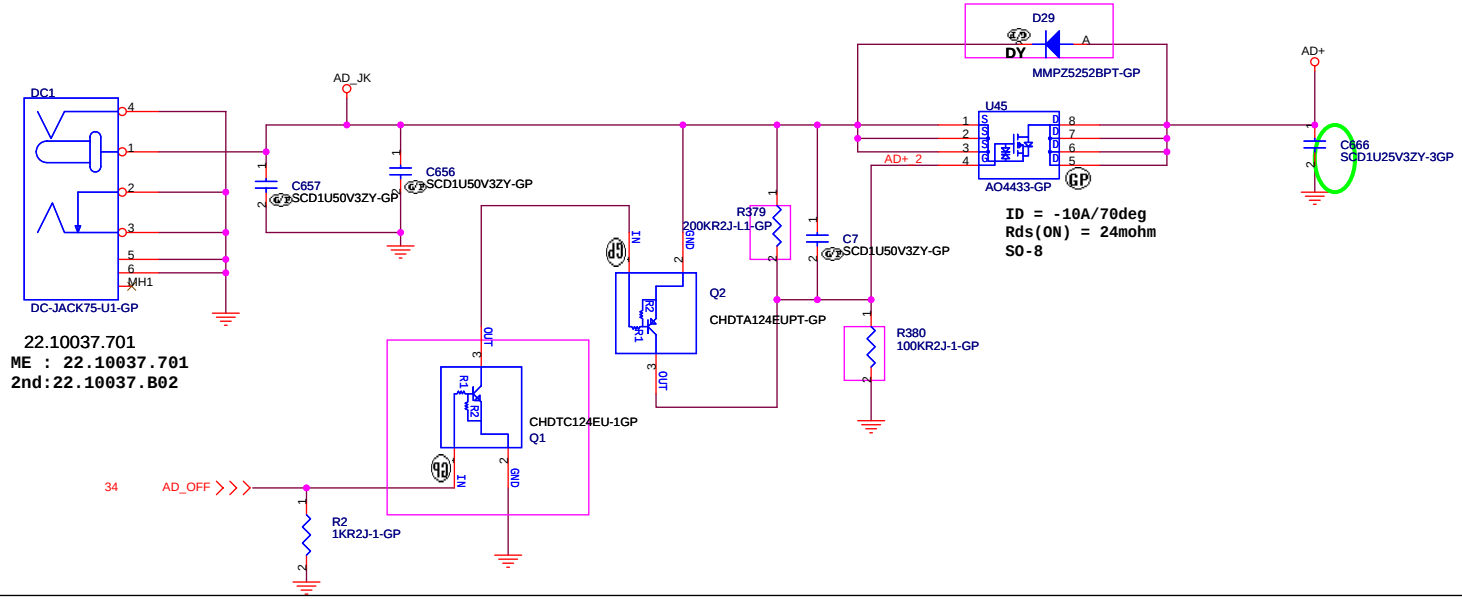
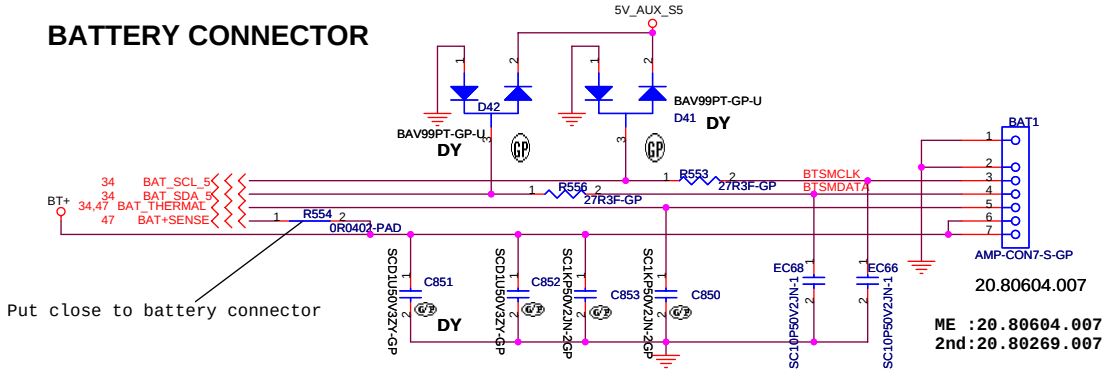
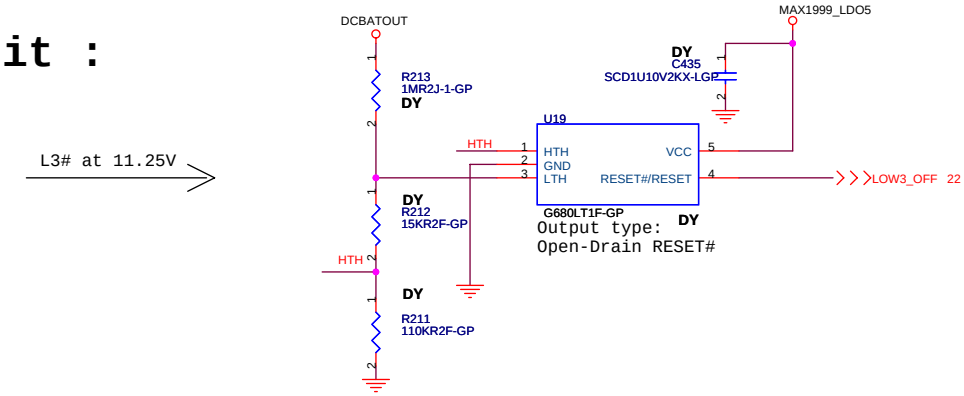
Adaptor in to generate DCBATOUT

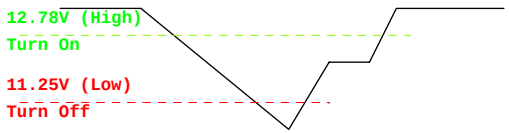


BATTERY CONNECTOR



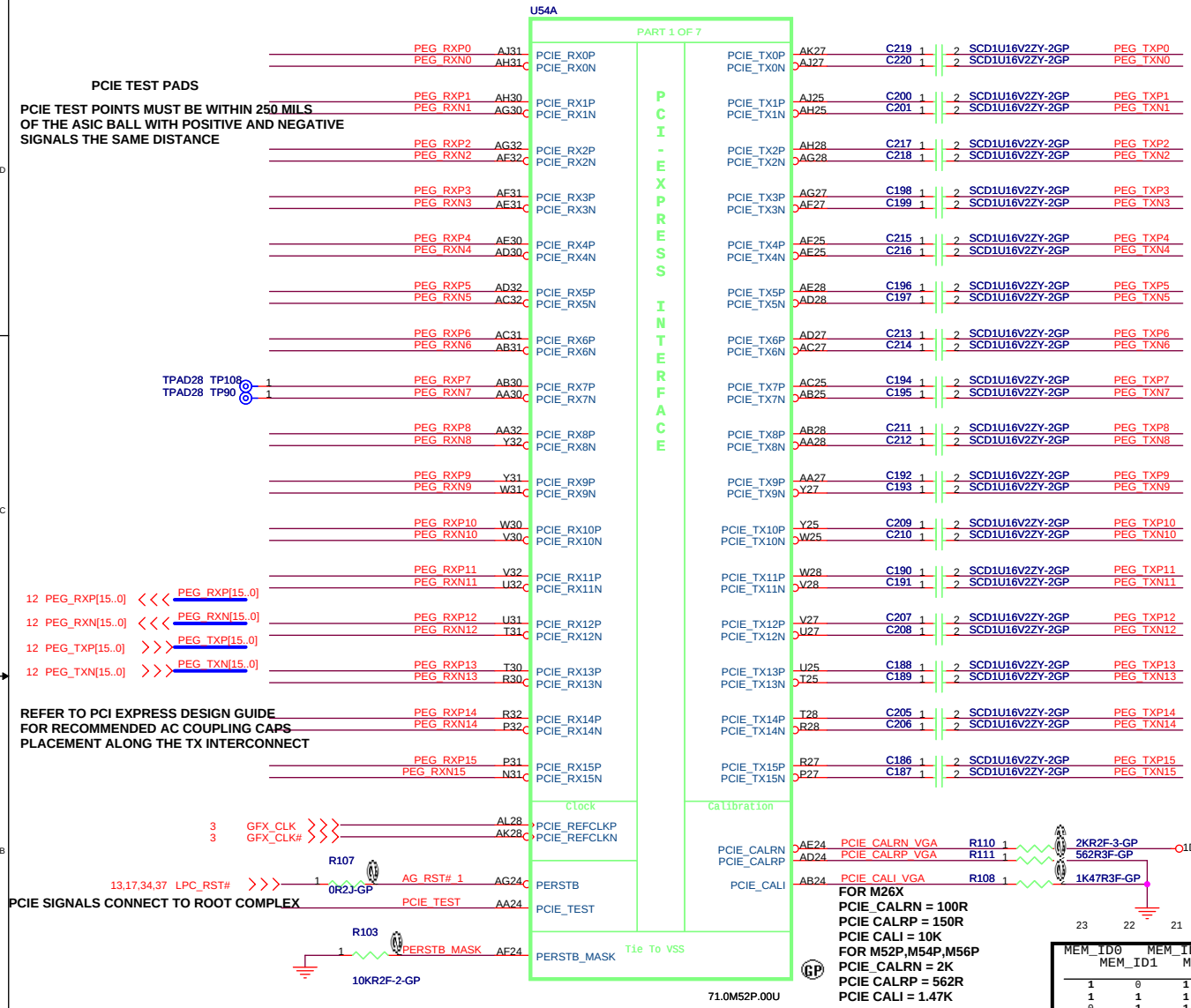
Low3 Circuit :



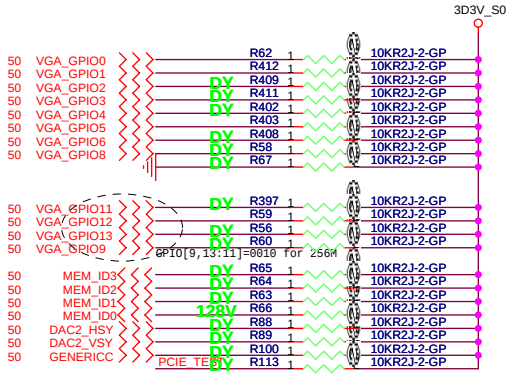


<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AD/BATT CONN	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 48 of 58	



STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE DEPENDS ON PCIE CHIPSET BEING USED FOR M26X,M5X INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS FOR M26X ONLY DO NOT INSTALL WITH INTEL 915PM CHIPSET	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NOT REVERSED LANE (M26X) NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE sets the desired PCIE PLL bandwidth for M5x parts.	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	INSTALL 10K RESISTORS
COMMON MODE RANGE RSVD	GPIO6	NORMAL RANGE (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	NO DEBUG ACCESS (M26X) DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO[9,13:11] GPIO[13:11]	SERIAL FLASH ROM TYPE (M26X,M52P,M54P,M56P) - SERIAL M25P10 ROM IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE SEE M26X,M54X,M56X DATA BOOK FOR MEMORY,FRAME BUFFER APERATURE SETTINGS	1011 TBD
MEM_TYPE	MEMID (3:0)	MEMORY TYPE AND SPEED SELECT	TBD
RSVD NO STRAP FUNCTION	H2SYNC V2SYNC GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	DO NOT INSTALL 10K RESISTORS
RSVD NO STRAP FUNCTION	PCIE_TEST	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	



MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3	MEM	SIZE	VENDOR	CHIPs
1	0	1	0	64M	16M*16	Infineon	x2
1	1	1	0	64M	16M*16	Hynix	x2
0	1	1	0	128M	16M*16	Samsung	x4
0	0	1	0	256M	32M*16	Samsung	x4
0	1	0	0	128M	16M*16	Infineon	x4
1	1	0	0	256M	32M*16	Infineon	x4
1	0	0	0	128M	16M*16	Hynix	x4
0	0	0	0	256M	32M*16	Hynix	x4

When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the frame buffer aperture size.
GPIO[13:12] = 00: 128M frame buffer, same as ROM strap 00
GPIO[13:12] = 01: 256M frame buffer, same as ROM strap 01
GPIO[13:12] = 10: 64M frame buffer, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M5X-P PCIE 1/4

Size: A3 | Document Number: AG1 | Rev: SA

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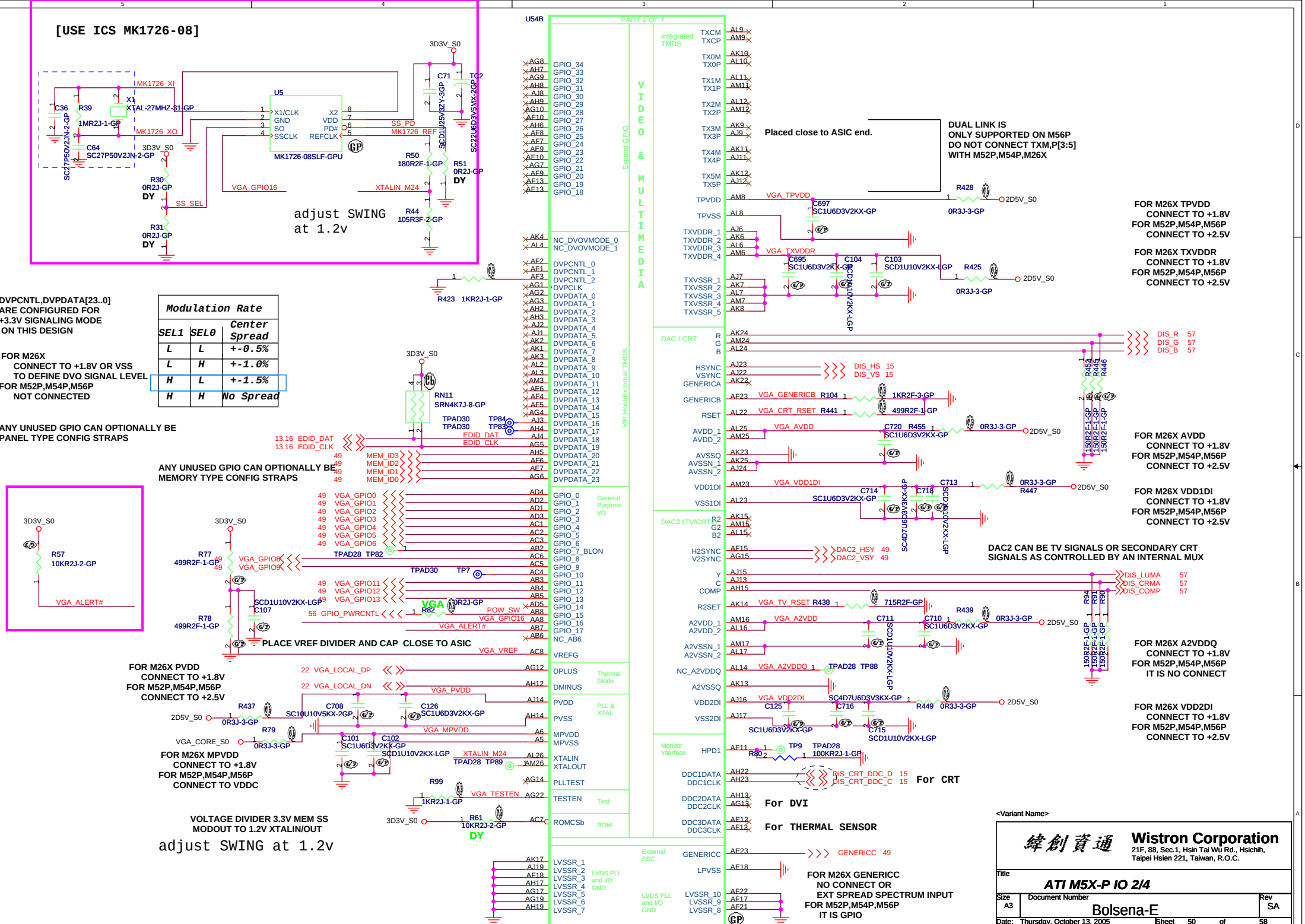
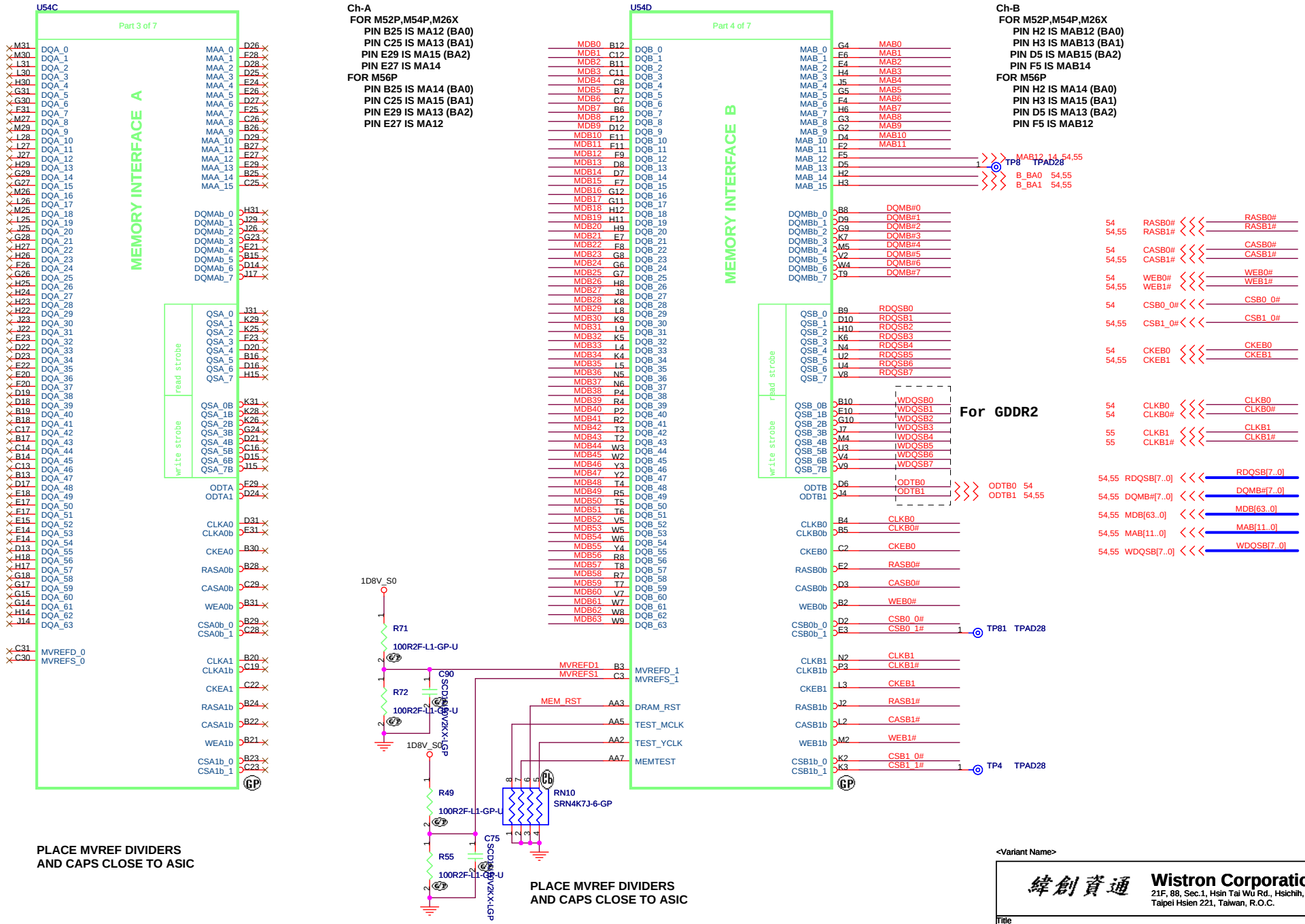
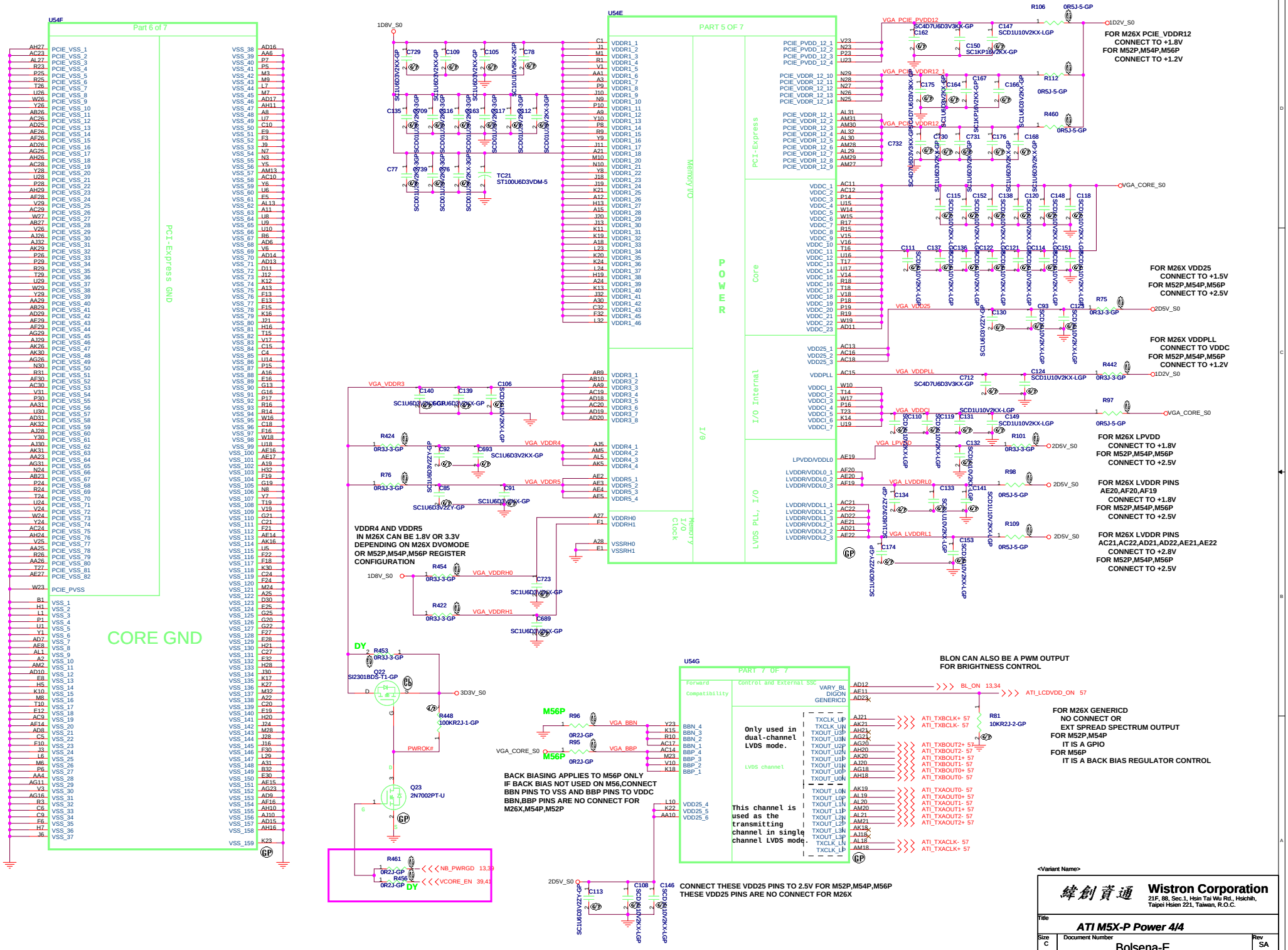


Modulation Rate		
SEL1	SEL0	Center Spread
L	L	+-0.5%
L	H	+-1.0%
H	L	+-1.5%
H	H	No Spread



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***ATI M5X-P MEM 3/4***
Size A3	Document Number Bolsena-E
Rev SA	
Date: Thursday, October 13, 2005	Sheet 51 of 58



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M5X-P Power 4/4

Size	Document Number	Rev
C	Bolsena-E	SA

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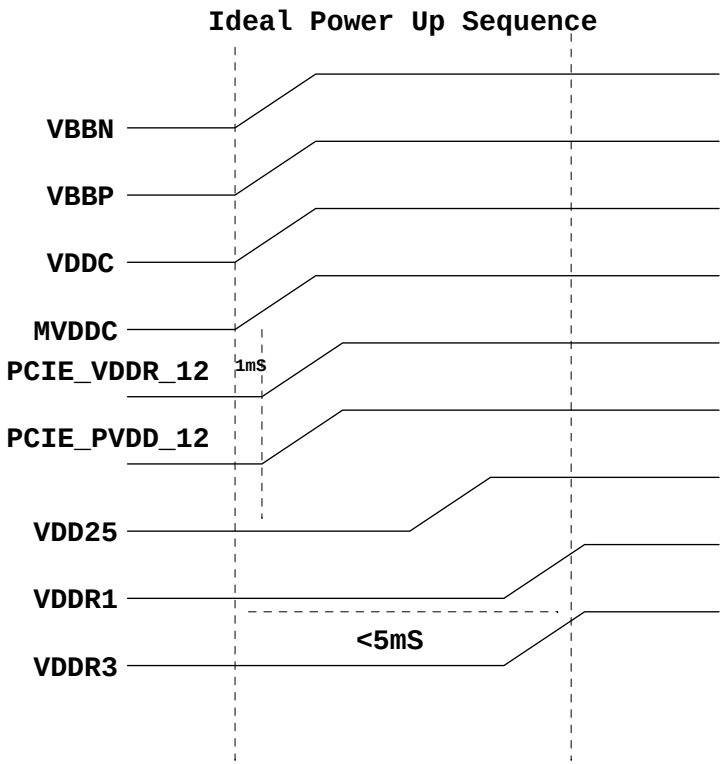

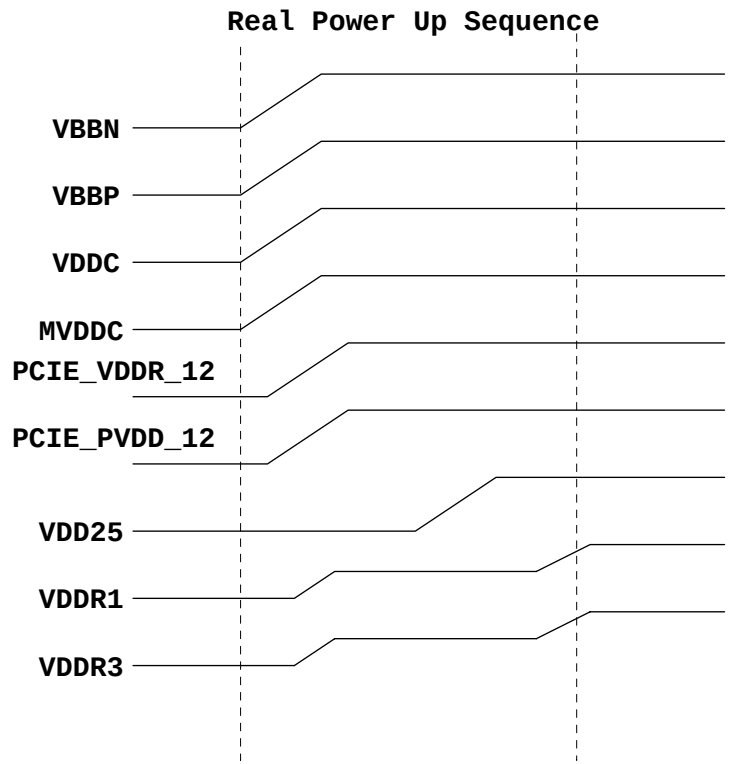

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

General Guidelines:

- **BBN and BBP must ramp up before or at the same time as VDDC but not after.**
- **VDDC and MVDDC must be ramped up first, followed by PCIE_VDDR_12, PCIE_PVDD12, VDD25, VDDR1 and VDDR3 (and other I/O powers).**
- **All powers must be ramped up within 5ms of each other (from the ramp of VDDC to 90% of VDDR3).**
- **VDD25 can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.**
- **The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD25 ->VDDC/MVDDC/BBN/BBP.**

Due to the level shifter design in the memory I/Os, in order to avoid over-stressing the thin oxide transistors when VDDR1 is powered on but VDDC is not, VDDC must ramp up before VDDR1. Similarly, VDDC must ramp up before VDDR3. The level shifter design is a function of the transistor types used in 90nm technology and of the voltage level support. The drawback of ramping up VDDC before the I/O voltages (such as VDDR1 and VDDR3) is that parasitic P/N junctions are forward biased, thus creating a conduction path. These conduction paths will pump up VDDR1 (from the memory IOs) and VDDR3 (from the GPIOs).

The real power up sequence will appear as follows:

Figure 2-2. Real Power Up Sequence

As long as MVDDC ramps up with VDDC, the pump voltage on VDDR1 should be all right since the DRAM spec will not be violated.

CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

<Variant Name>

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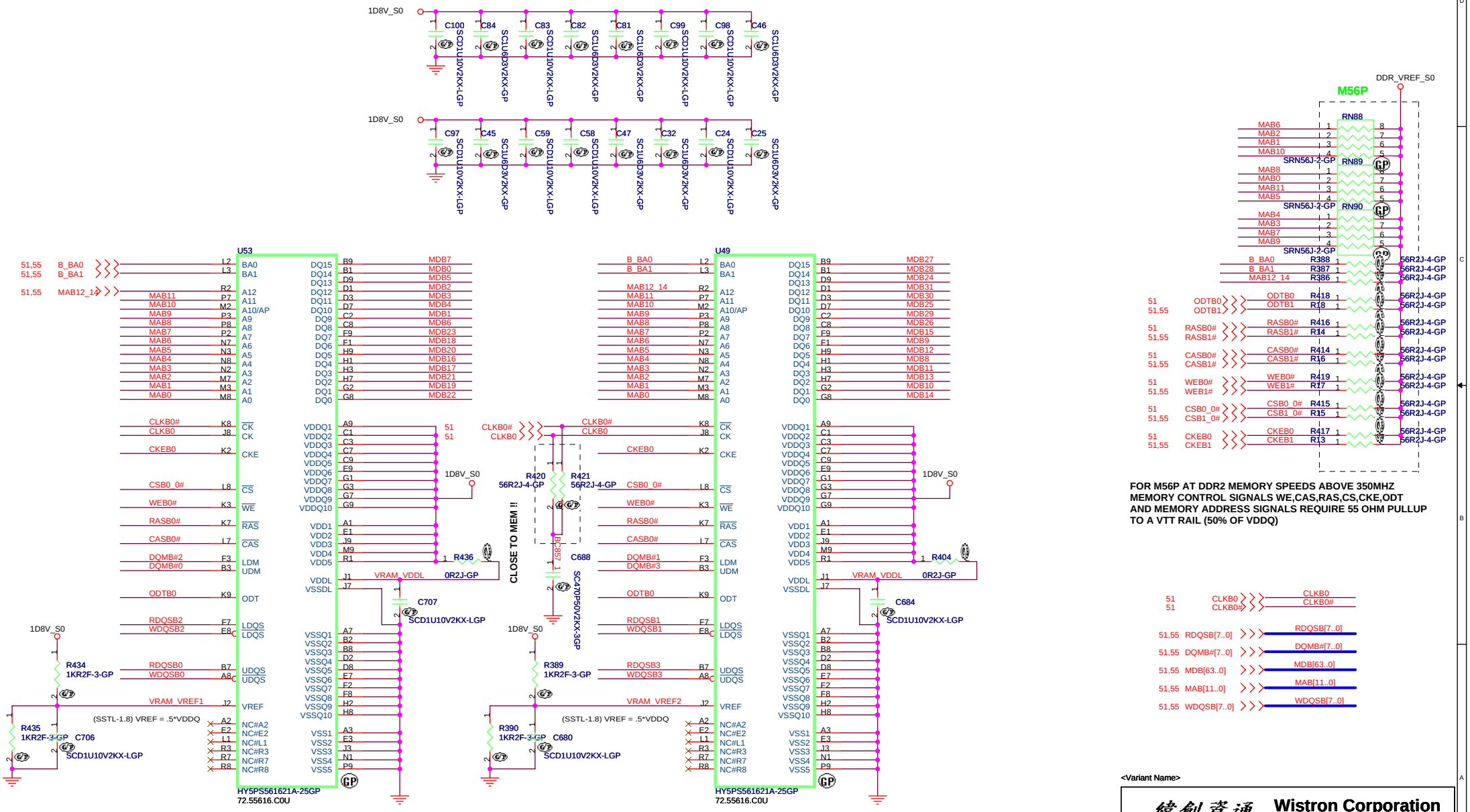
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ATI M5X-P POWER SEQUENCE***

Size: A3 | Document Number: **Bolsena-E** | Rev: **SA**

Date: Thursday, October 13, 2005 | Sheet 53 of 58

CHAN B DDR2 84BGA 32MX16 MEMORY



72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGA(16M*16, 400Mhz)
72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M*16, 400Mhz)

<Variant Name>

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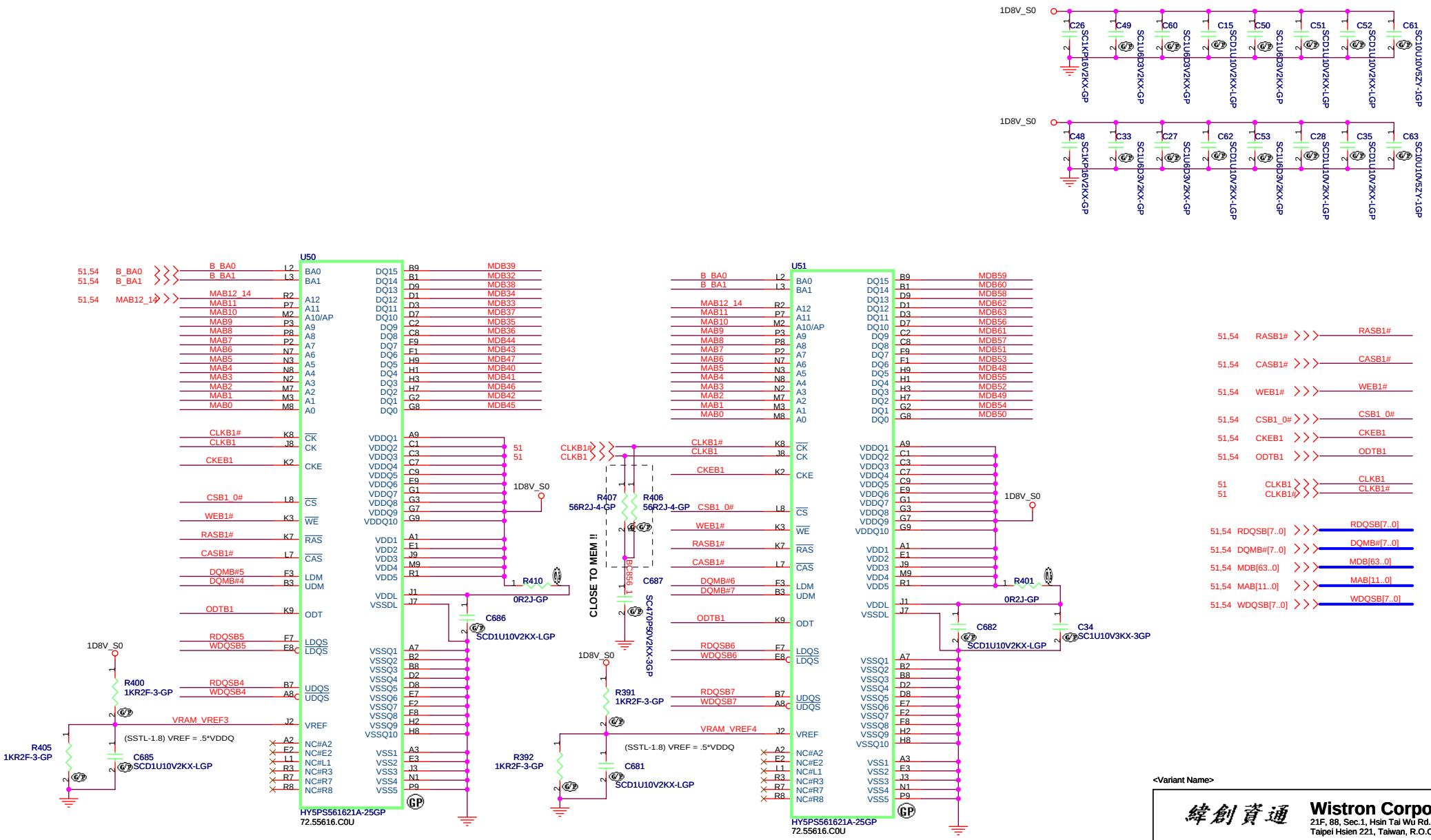
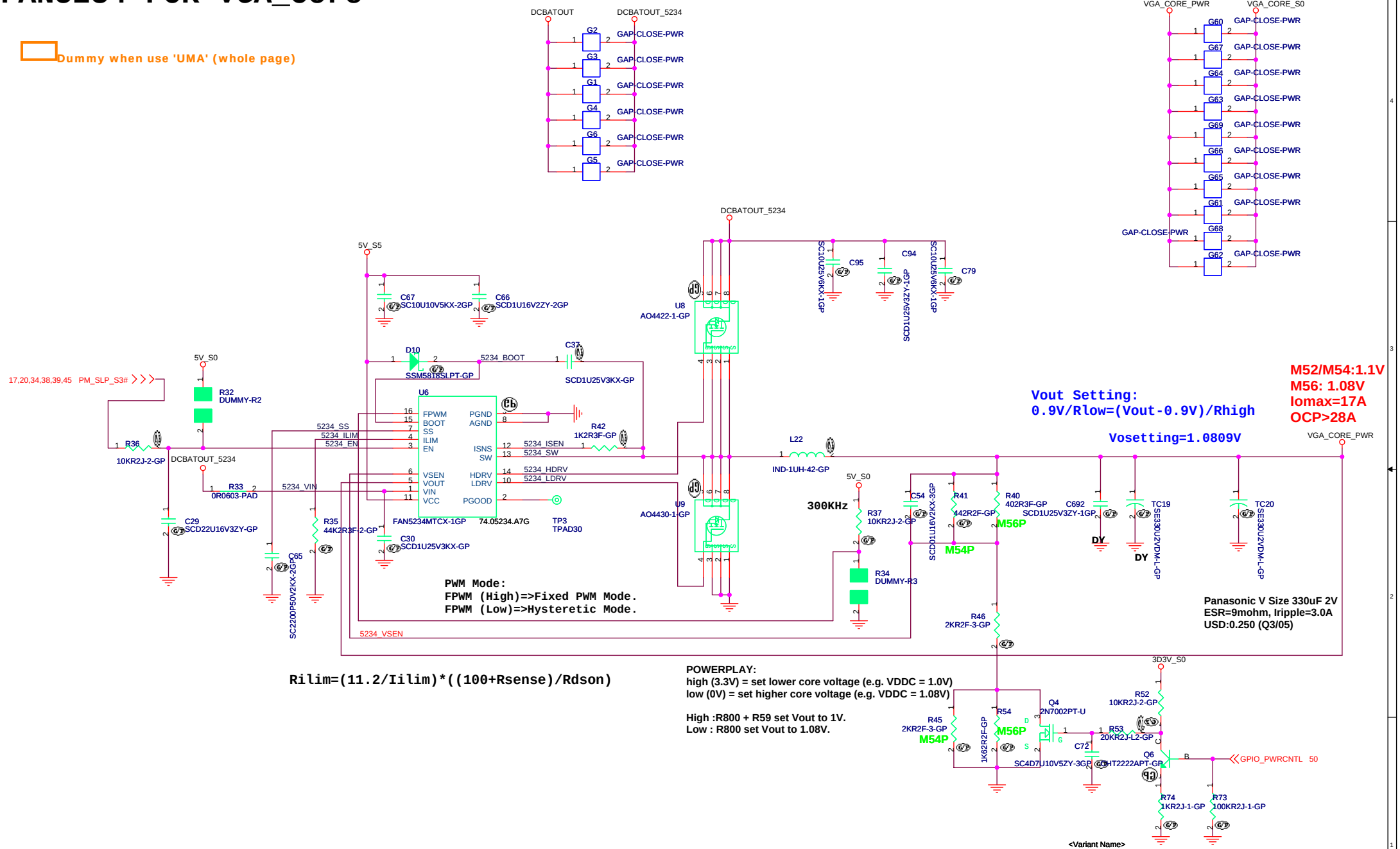
Title	***VRAM 1/2***
Size A3	Document Number Bolsena-E
Rev SA	
Date: Thursday, October 13, 2005	Sheet 54 of 58



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM 2/2***	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 55 of 58	

FAN5234 FOR VGA_Core



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<Variant Name>

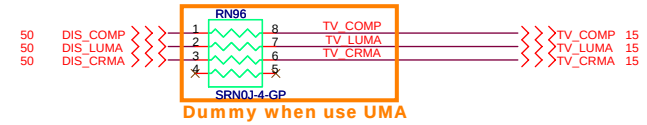
Title: VGA CORE 1D1V

Size: A3 | Document Number: Bolsena-E | Rev: SA

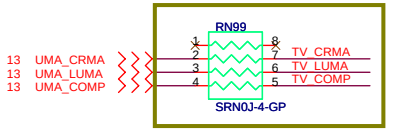
Date: Thursday, October 13, 2005 | Sheet 56 of 58

TV SWITCH

Function	S
A to B0	L
A to B1	H

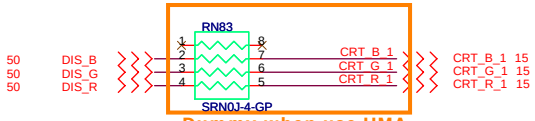


Dummy when use UMA



Dummy when use Discrete

-1 0308



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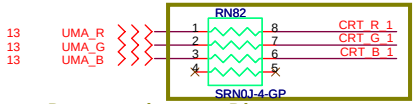

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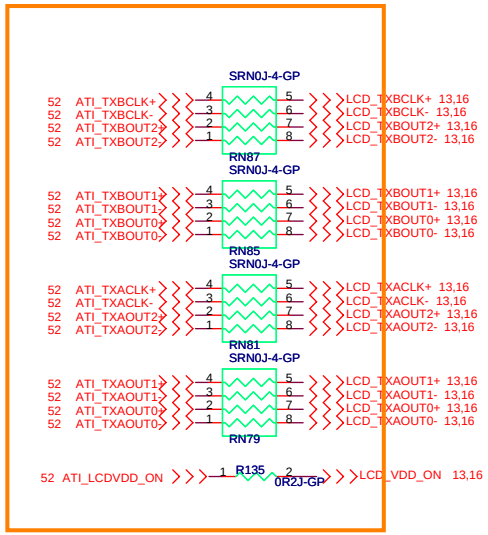

<Variant Name>

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Title: VGA SELECTOR

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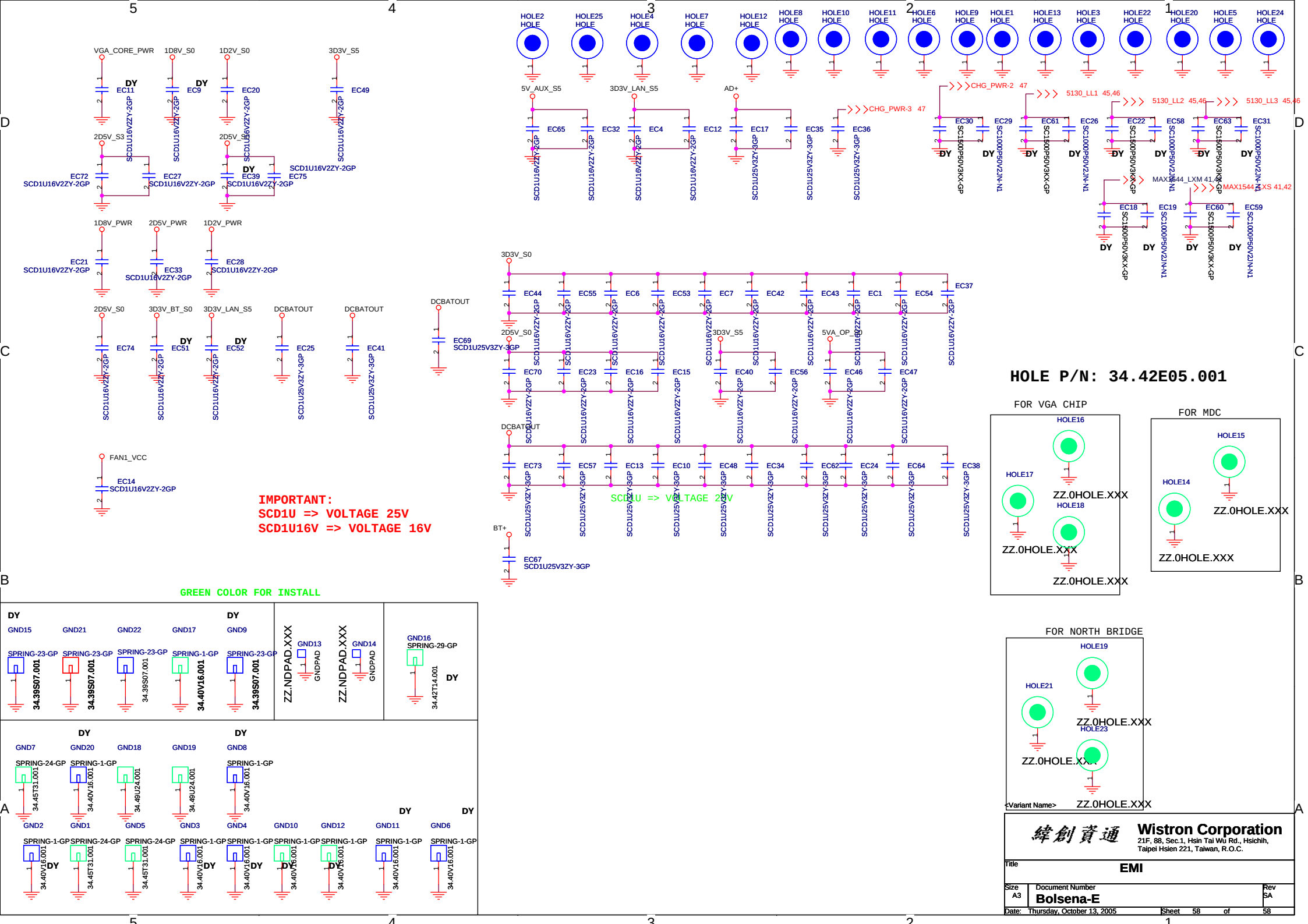
HOLE P/N: 34.42E05.001
FOR VGA CHIP
FOR MDC
FOR NORTH BRIDGE
ZZ.0HOLE.XXX
IMPORTANT:
SCD1U => VOLTAGE 25V
SCD1U16V => VOLTAGE 16V
SCD1U => VOLTAGE 25V
GREEN COLOR FOR INSTALL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI
Size
A3
Document Number
Bolsena-E
Rev
SA
Date: Thursday, October 13, 2005
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